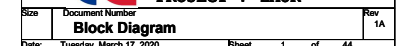


# 01



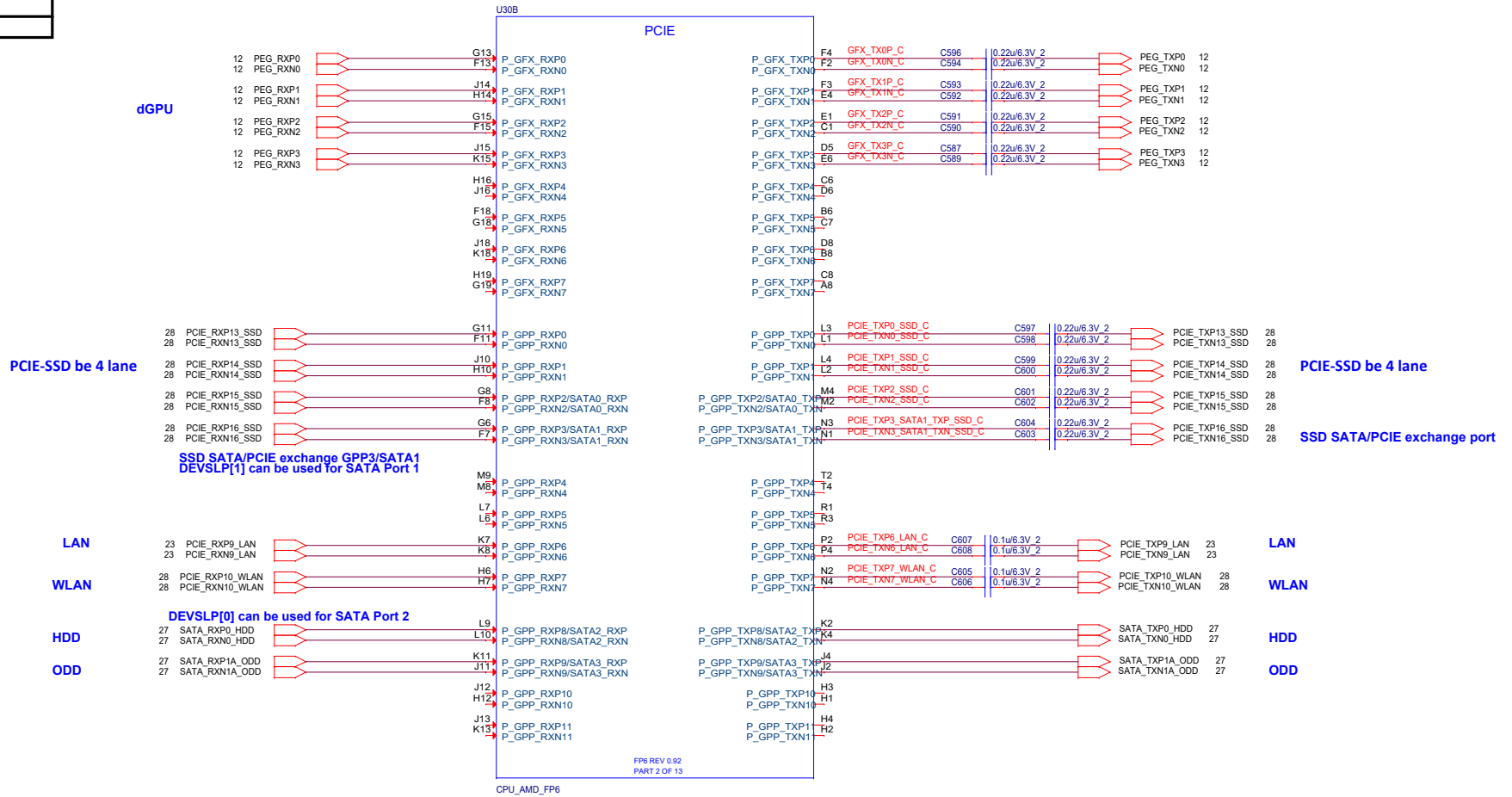


## APU PCIE

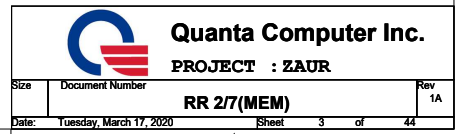
AMD APU	TOP BSQ	QBCON

PCIe Port	Function
PCIe_0	SSD_PCIe
PCIe_1	SSD_PCIe
PCIe_2	SSD_PCIe
PCIe_3	SSD_PCIe
PCIe_4	NA
PCIe_5	NA
PCIe_6	LAN
PCIe_7	WLAN

SATA Port	Function
SATA_1	M.2_SSD
SATA_2	HDD
SATA_3	ODD



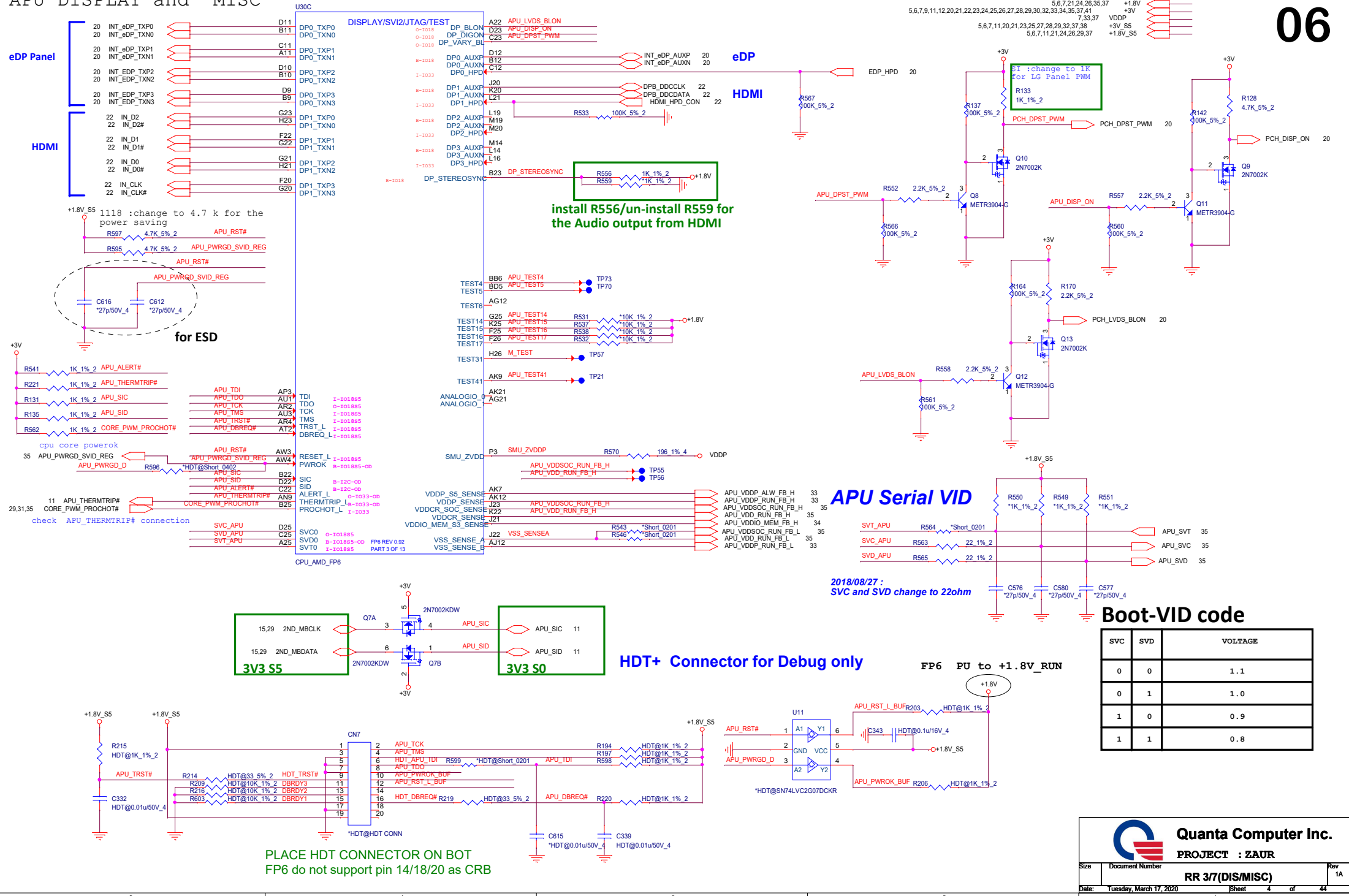






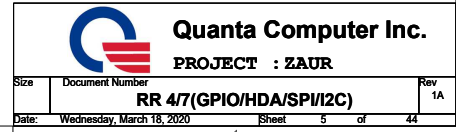
# APU DISPLAY and MISC

06

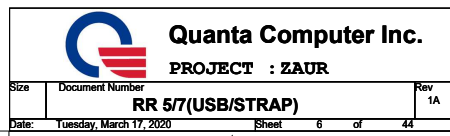




## 07





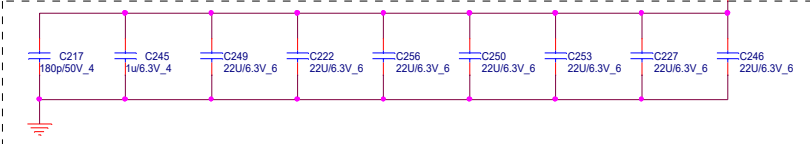




# APU POWER

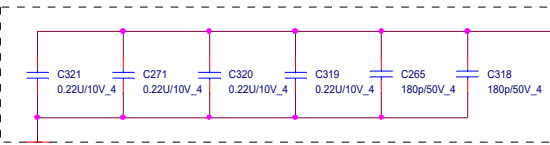
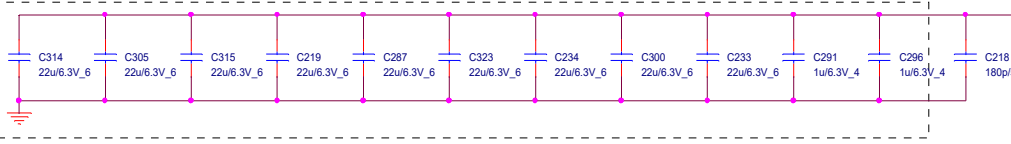
09

## BOTTOM SIDE DECOUPLING UNDER APU



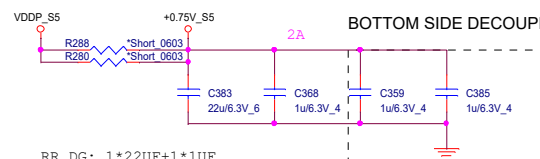
RR DG: 9\*22UF+2\*1UF+4\*0.22uf+3\*180PF

## BOTTOM SIDE DECOUPLING UNDER APU



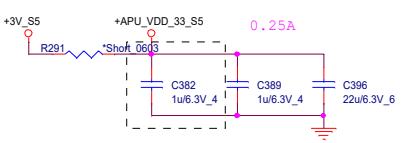
If the VSS plane is cut to create a VDDIO\_MEM\_S3 plane, ceramic capacitors with NP0 or COG dielectric are connected across the VDDIO\_MEM\_S3 and VSS plane split.

RR DG: 1\*22UF+3\*1UF



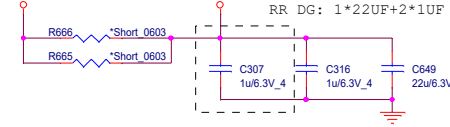
## BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1\*22UF+2\*1UF



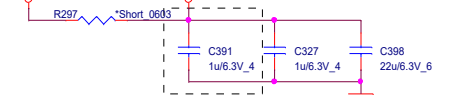
## BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1\*22UF+2\*1UF

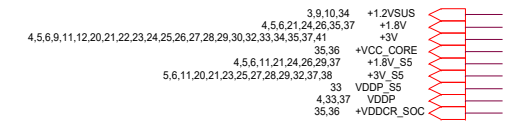
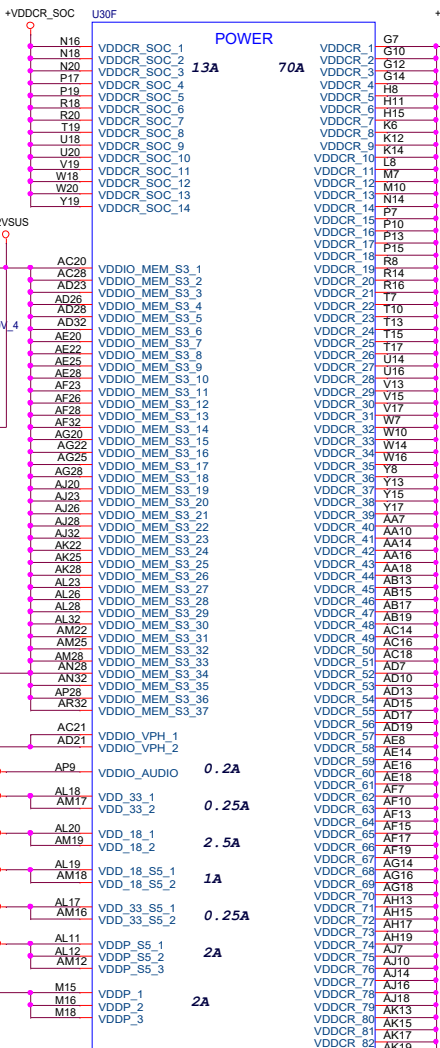


## BOTTOM SIDE DECOUPLING UNDER APU

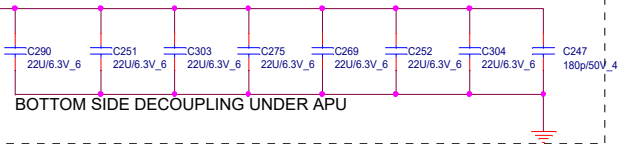
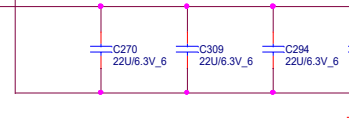
RR DG: 1\*22UF+2\*1UF



## BOTTOM SIDE DECOUPLING UNDER APU

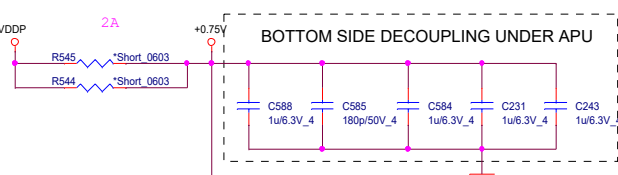


RR DG: 16\*22UF+1\*180PF

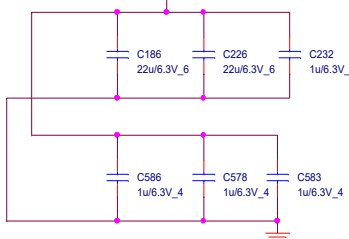


## BOTTOM SIDE DECOUPLING UNDER APU

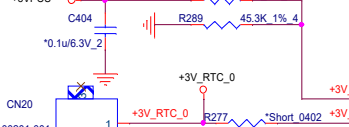
RR DG: 2\*22UF+8\*1UF+1\*180PF



## BOTTOM SIDE DECOUPLING UNDER APU



## BOTTOM SIDE DECOUPLING UNDER APU



## BOTTOM SIDE DECOUPLING UNDER APU

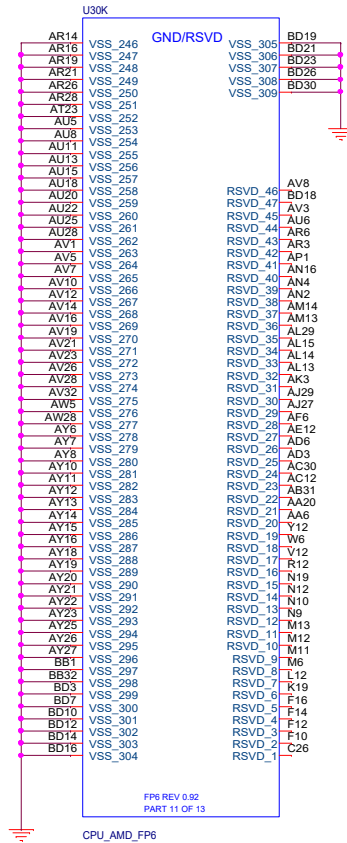
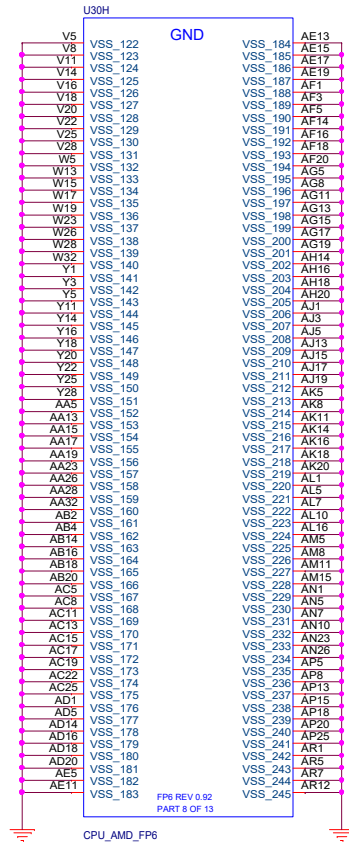
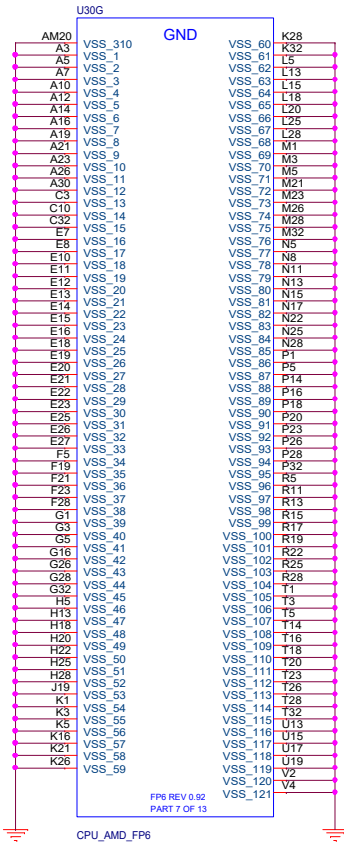


## RTC Circuitry(RTC)

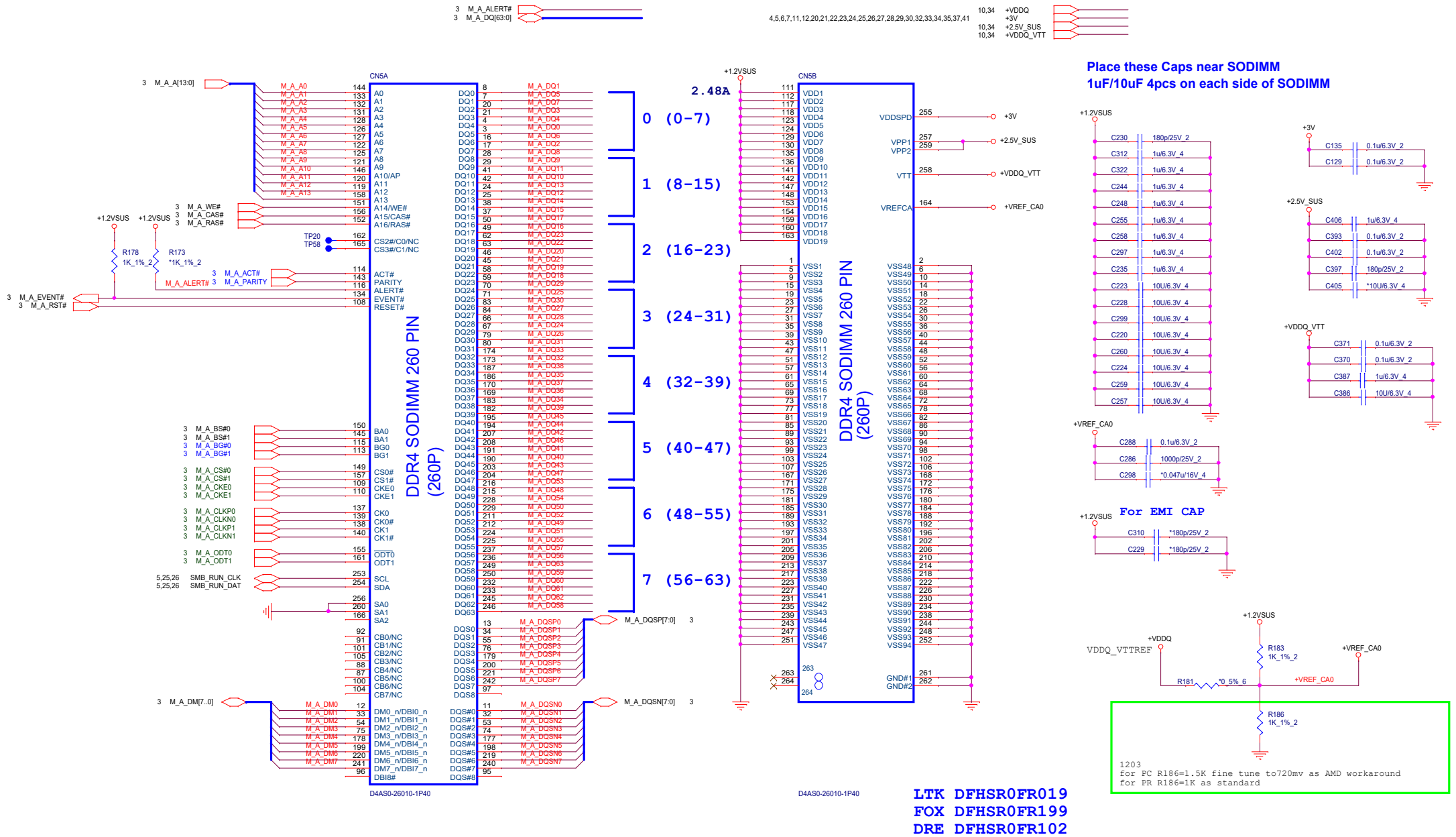
RTC Power trace width 20mils. Coin Battery: Connected to a +3.3V from coin battery through a series resistor of: 1K

<b>Quanta Computer Inc.</b> <b>PROJECT : ZAUR</b>		
Size	Document Number	Rev
	<b>RR 67(POWER)</b>	<b>1A</b>
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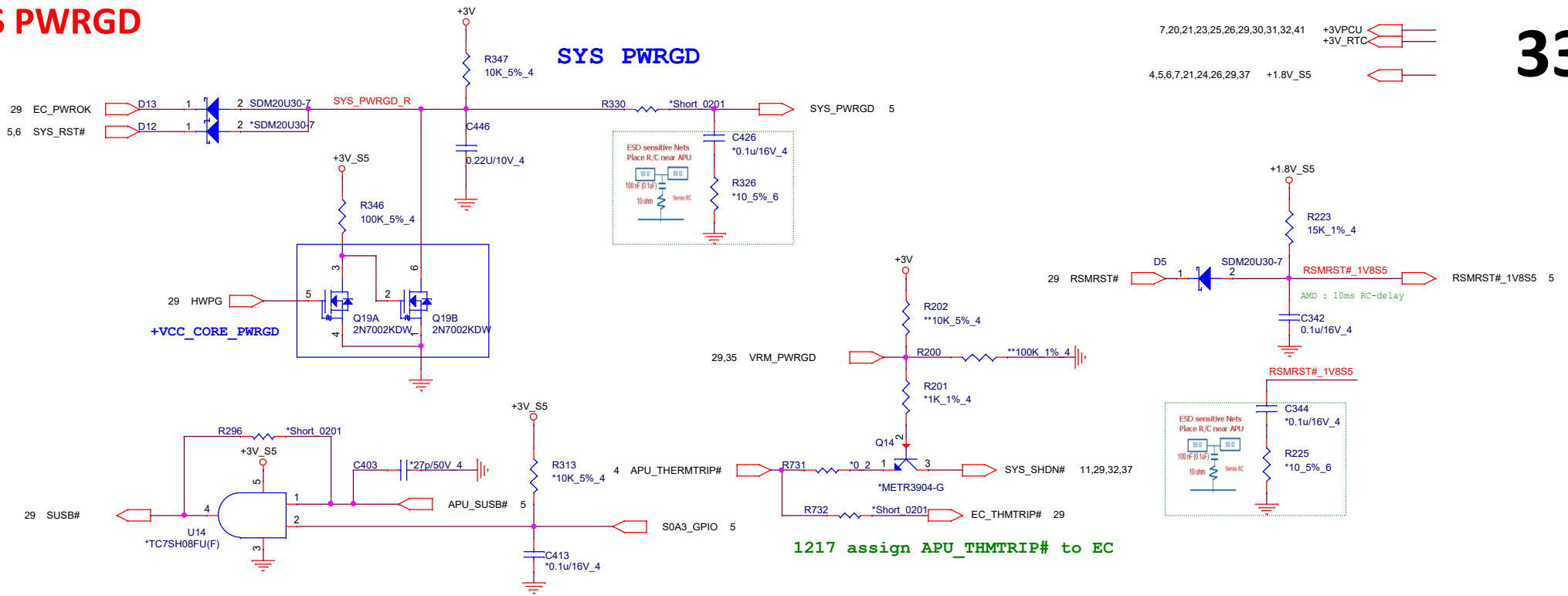




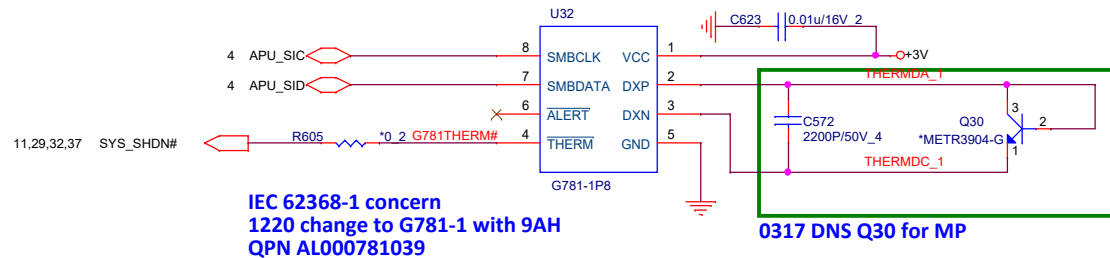


# SYS\_PWRGD

## SYS\_PWRGD



## Address 9AH



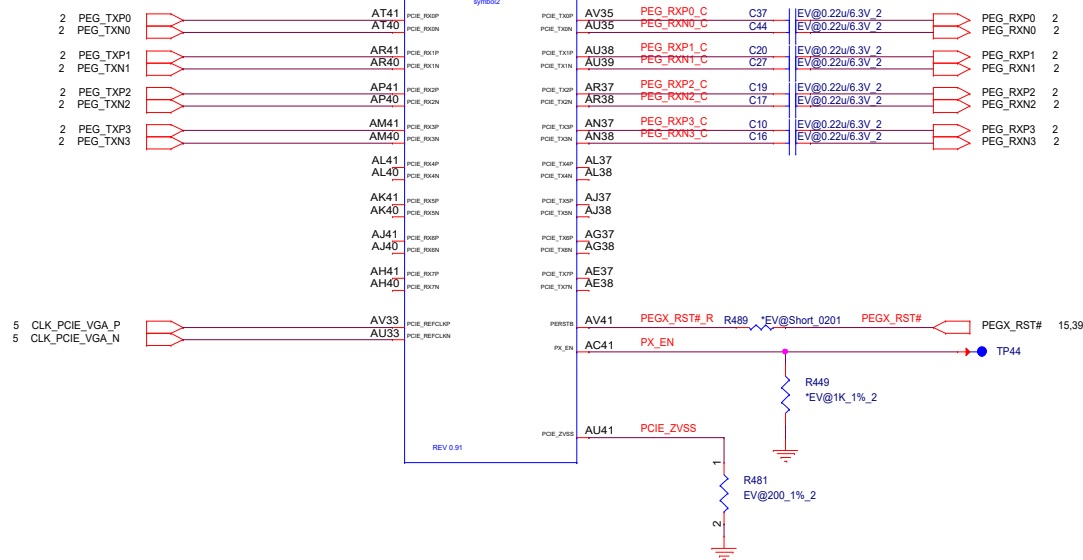
Quanta Computer Inc.

PROJECT : ZAUR

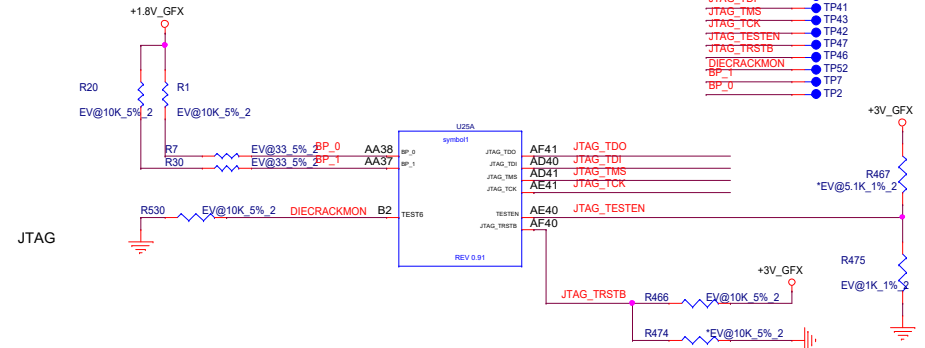
Size	Document Number	Rev
	RR SYSPWRGD/ThermalSensor	1A
Date:	Tuesday, March 17, 2020	Sheet 11 of 44

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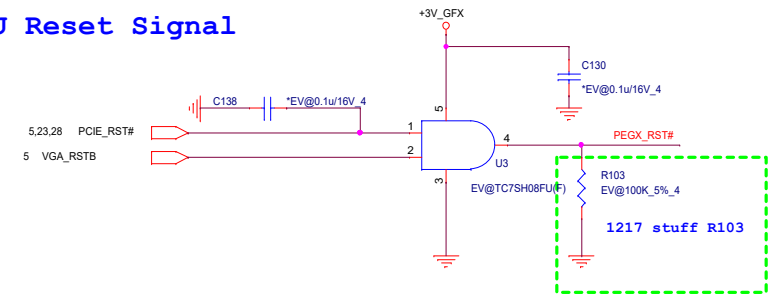


## debug port

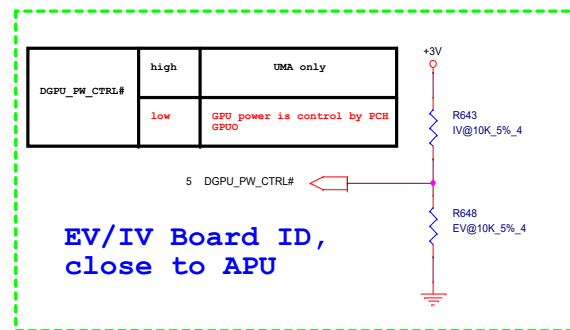
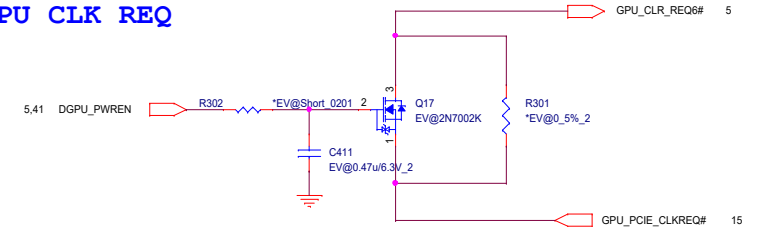


AMD Change the PU and PD resistors of JTAG\_TRSTB to 10K and mounting PU resistor  
AMD change the PU resistor of JTAG\_TESTEN to 5.1K and keeping reserved.

## GPU Reset Signal



## GPU CLK REQ

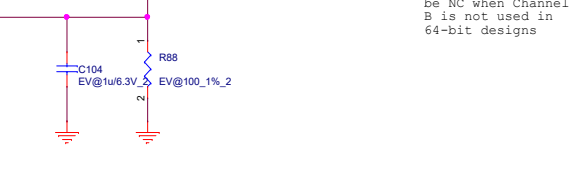
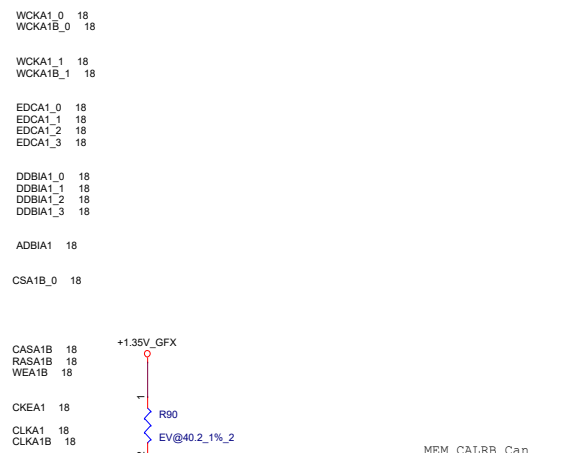
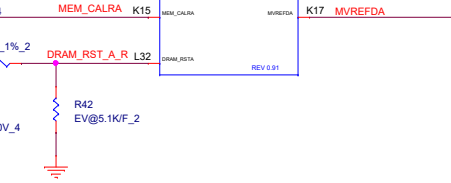
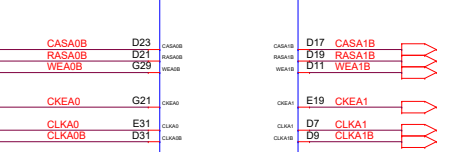
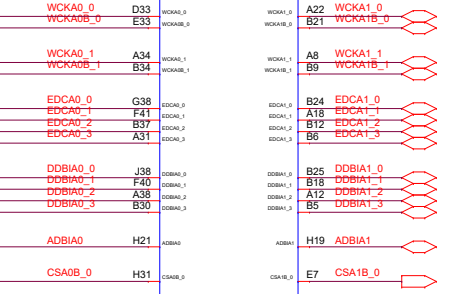
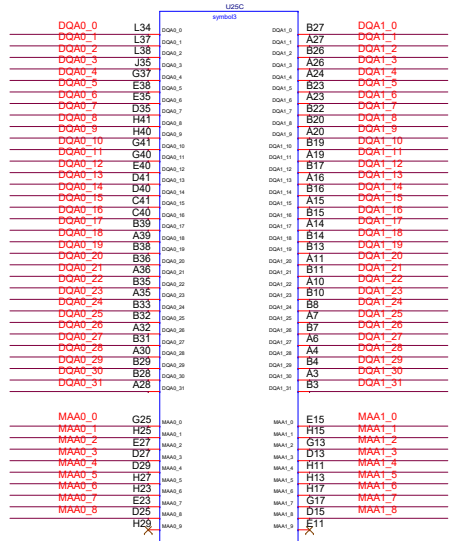


EV/IV Board ID,  
close to APU

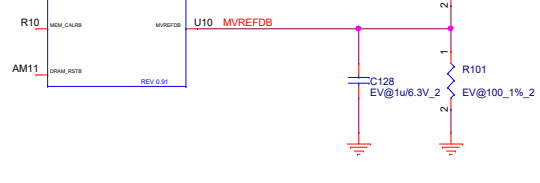
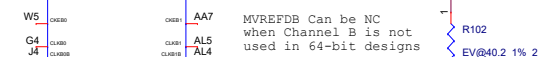
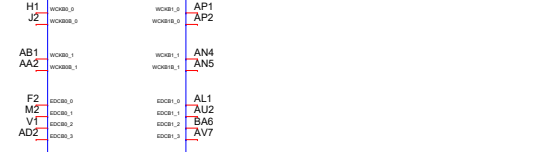
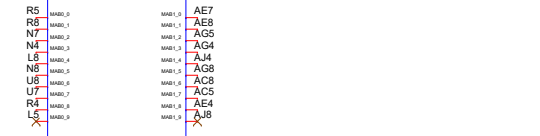
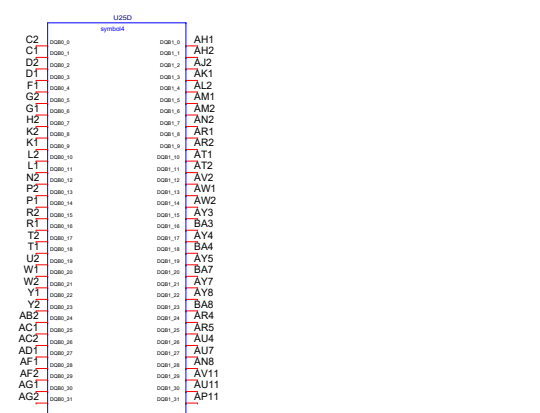


18 DQA0\_[31:0] 18  
18 MAA0\_[8:0] 18

DQA1\_[31:0] 18  
MAA1\_[8:0] 18



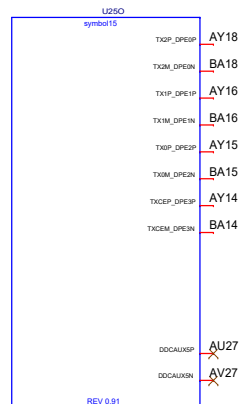
MEM CALRB Can be NC when Channel B is not used in 64-bit designs



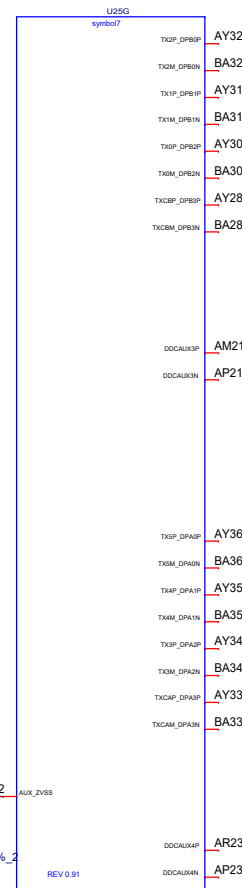
MVREFDB Can be NC when Channel B is not used in 64-bit designs



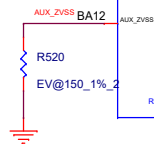
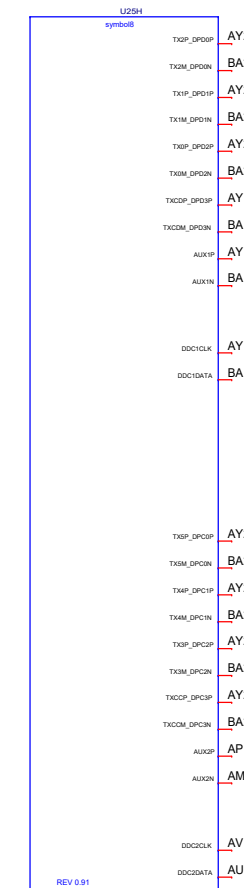
# ASIC - TMDP (E)




# ASIC - TMDP (A/B)

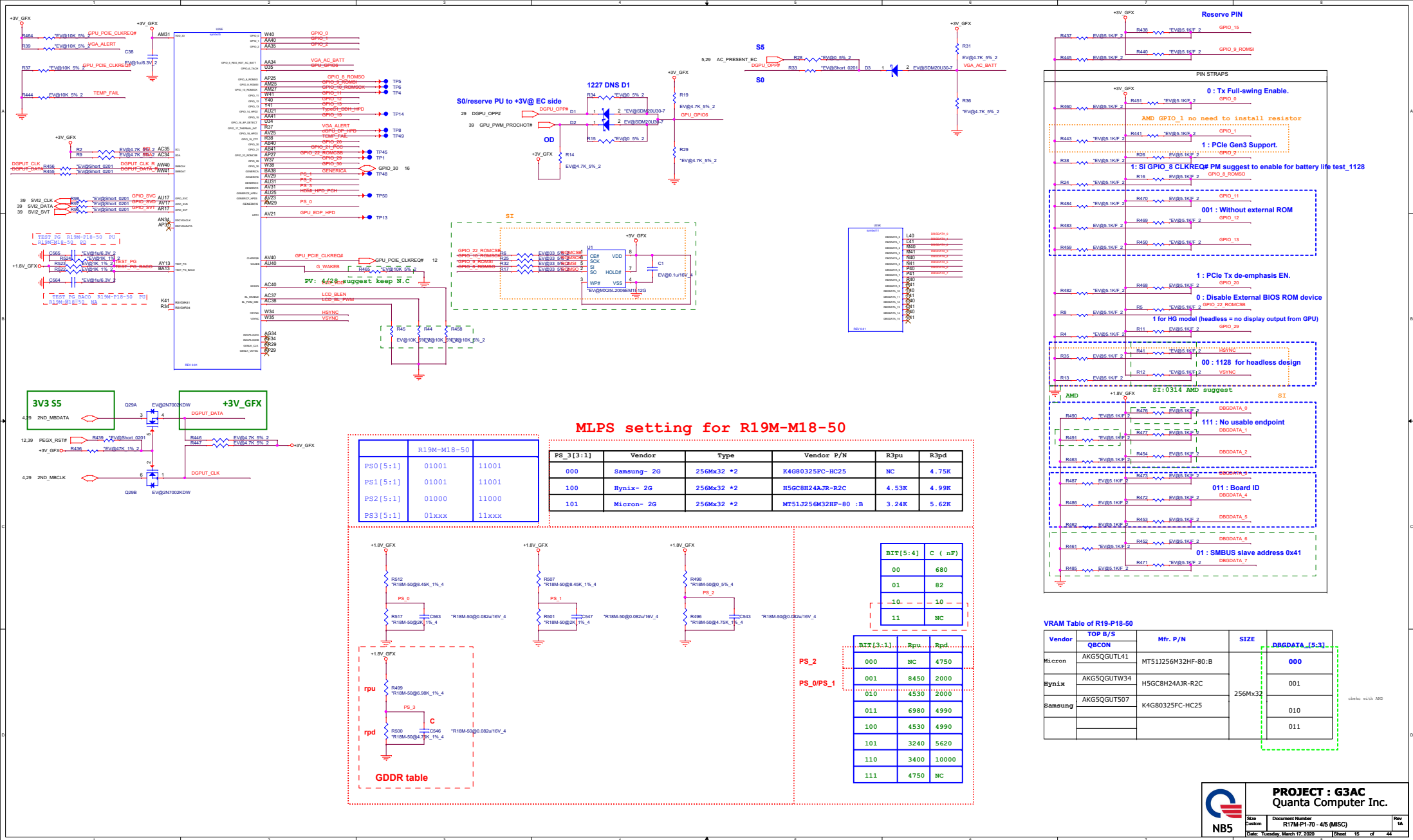


# ASIC - TMDP (C/D)

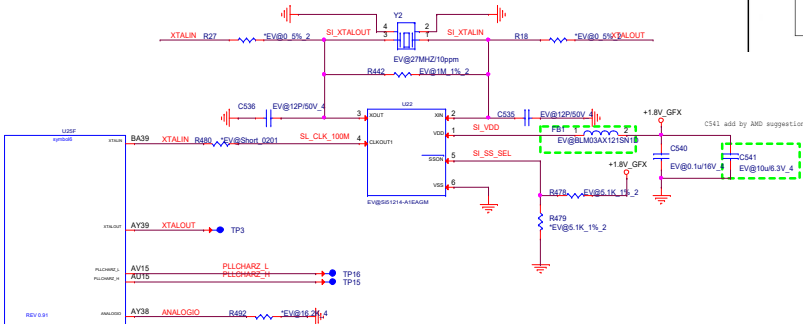
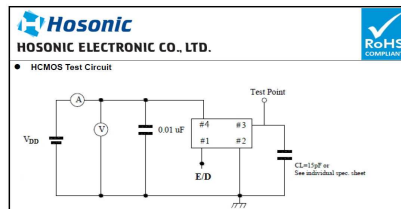
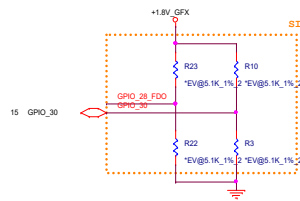
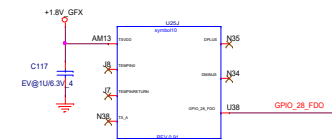


	<b>PROJECT : G3AC</b> <b>Quanta Computer Inc.</b>	
	Size A3	Document Number R17M-P1-70- 3/5 (Display)
	Date: Tuesday, March 17, 2020	Sheet 14 of 44



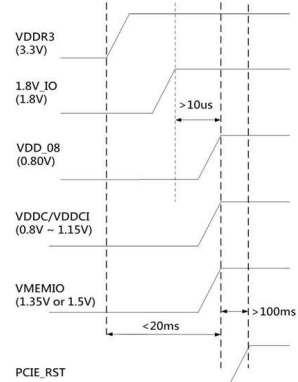




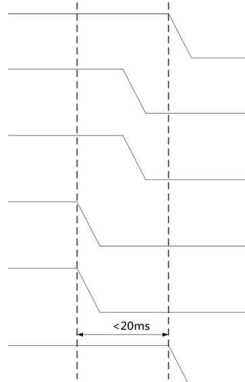


R10M-G1-10 Power up sequence for you refer:

## POWER UP

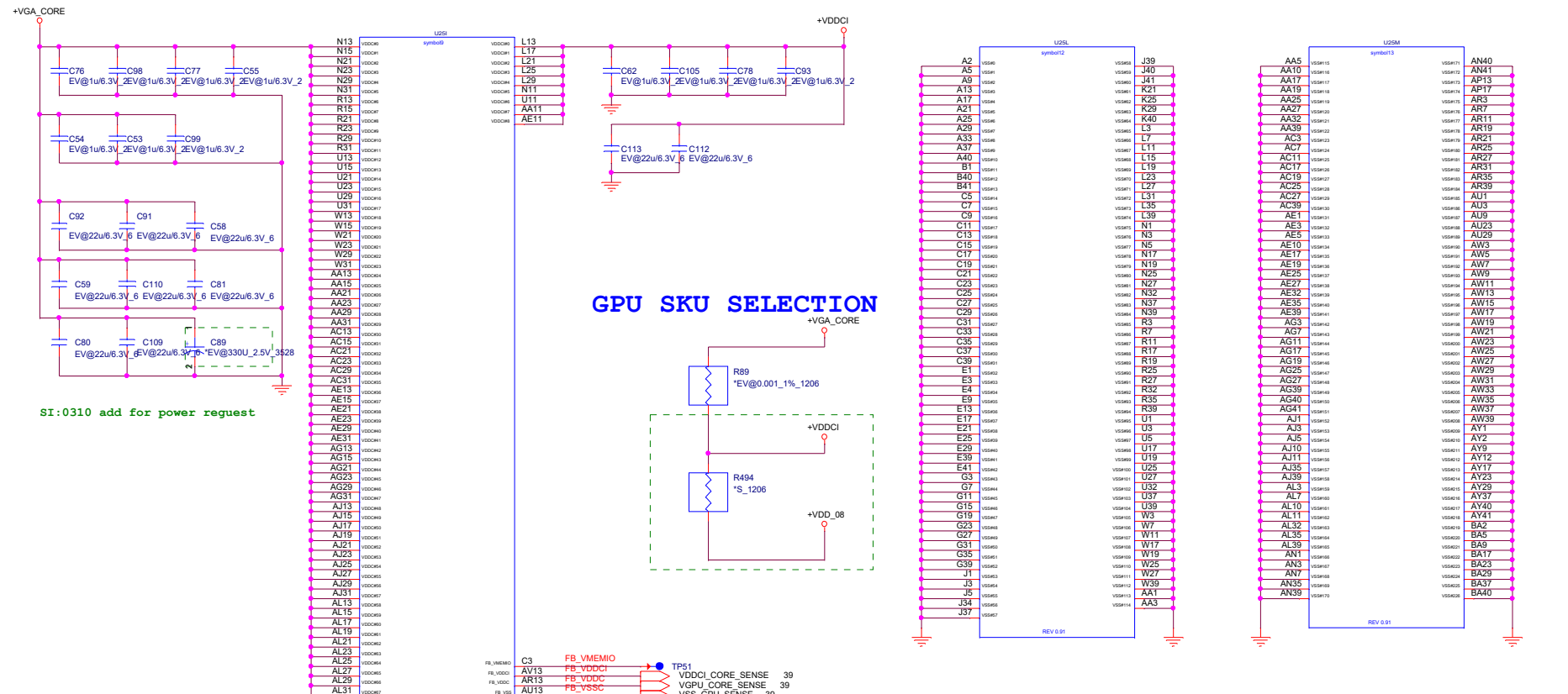


## POWER DOWN

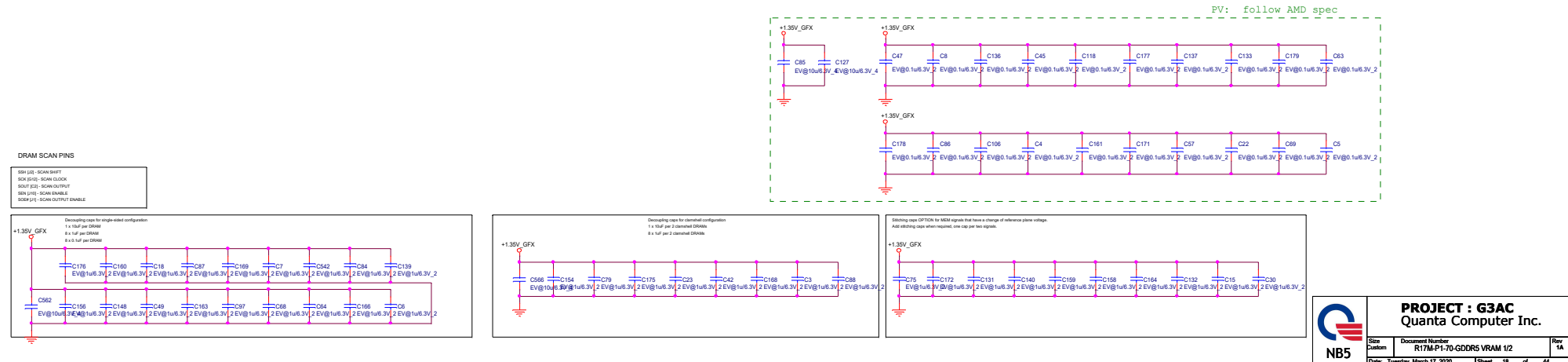
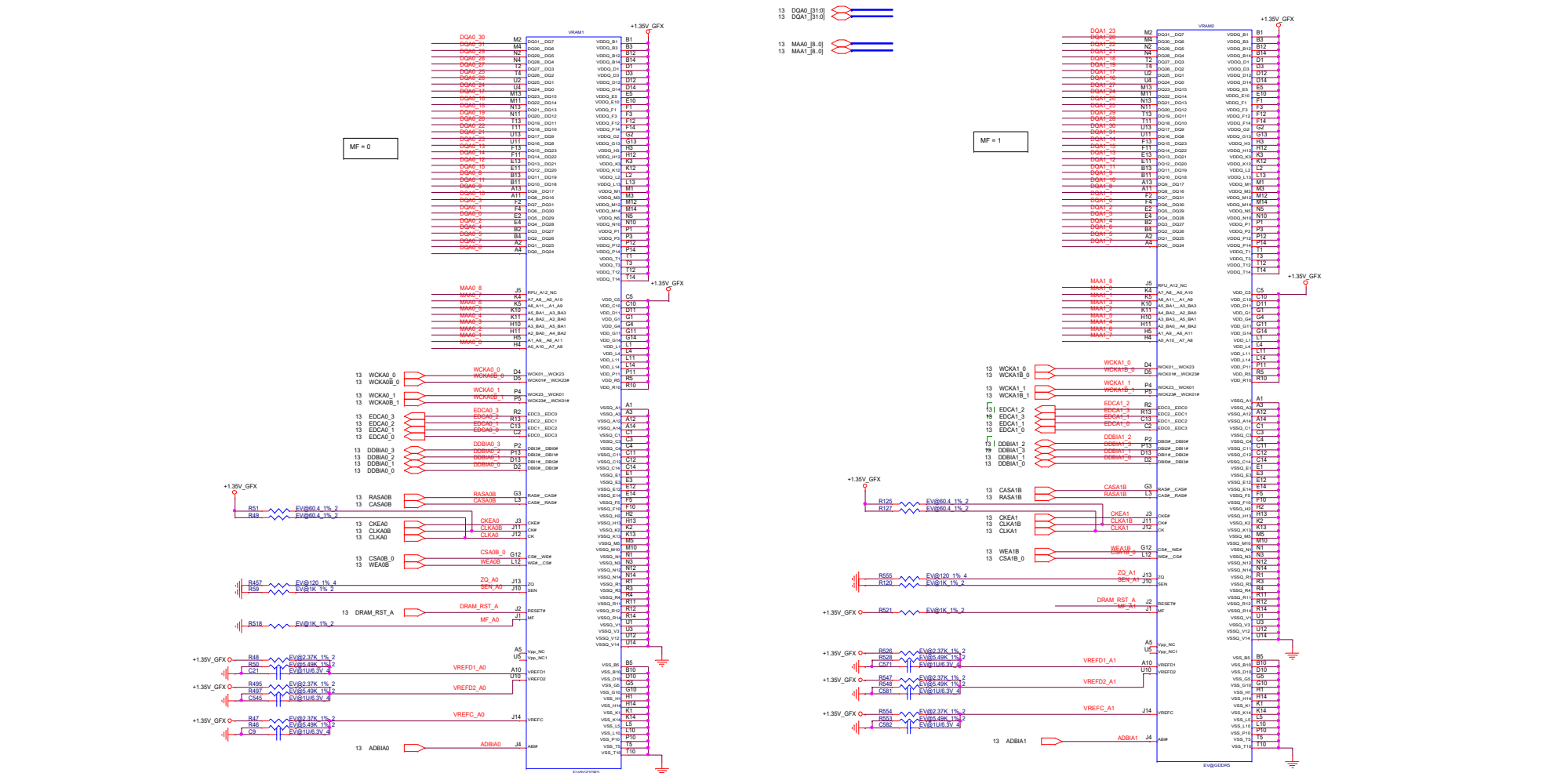


AMD GPIO Strapping	Setting	Name	Description
GPIO 29	Pull low 10K ohm	BIF_VGA_DIS	0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).
GPIO 20	Pull up 10K ohm	TX_DEEMPH_EN	PCI Express transmitter deemphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.
GPIO 0	Pull up 10K ohm	TX_HALF_SWING	Controls the transmitter full/half swing mode. 0: The transmitter full swing is enabled. 1: The transmitter half swing is enabled.
GPIO 22	Pull low 10K ohm	BIOS_ROM_EN	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device.
GPIO 11	Pull up 10K ohm	ROM_CONFIG[2:0]	b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. GPIO_1[3:2:1]=001=256MB
GPIO 12	Pull low 10K ohm		
GPIO 13	Pull low 10K ohm		
Hsync	NC	Reserve	Reserve
Vsync	NC	Reserve	Reserve
DBGDATA2	Pull up 10K ohm	AUD_PORT_CONN [2:0]	Determine the maximum number of digital display audio endpoints 101: Two usable endpoints
DBGDATA1	Pull low 10K ohm		
DBGDATA0	Pull up 10K ohm		
GPIO 1	Pull up 10K ohm	SMBUS_ADDR	Provide a strap option to change the SMBUS slave address of the GPU. 0: 0x40 1: 0x41
GPIO 2	Pull up 10K ohm	BIF_GEN3_EN_A	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.
GPIO 8	connect CLKREQ#_GPU and add pull up / down resistor	BIF_CLK_PM_EN (Reserve)	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.
WAKEB	Pull low 10K ohm	OBFF	0: Disable
SVI2_SVC	Pull up 1Kohm	Boot up voltage	SVC:SVDD=[1:0]=0.90V
SVI2_SVD	Pull low 1K ohm		



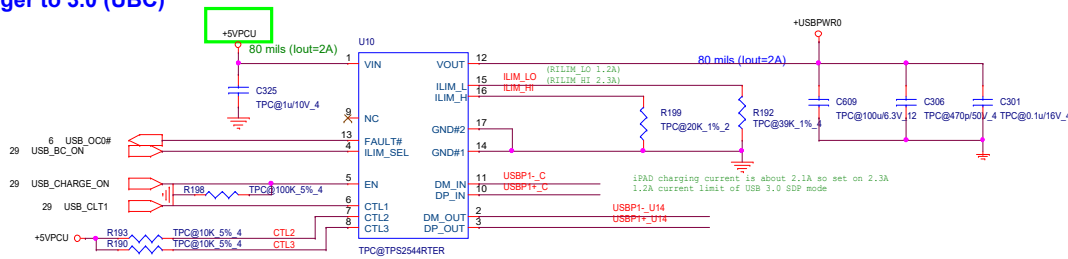








USB Charger to 3.0 (UBC)

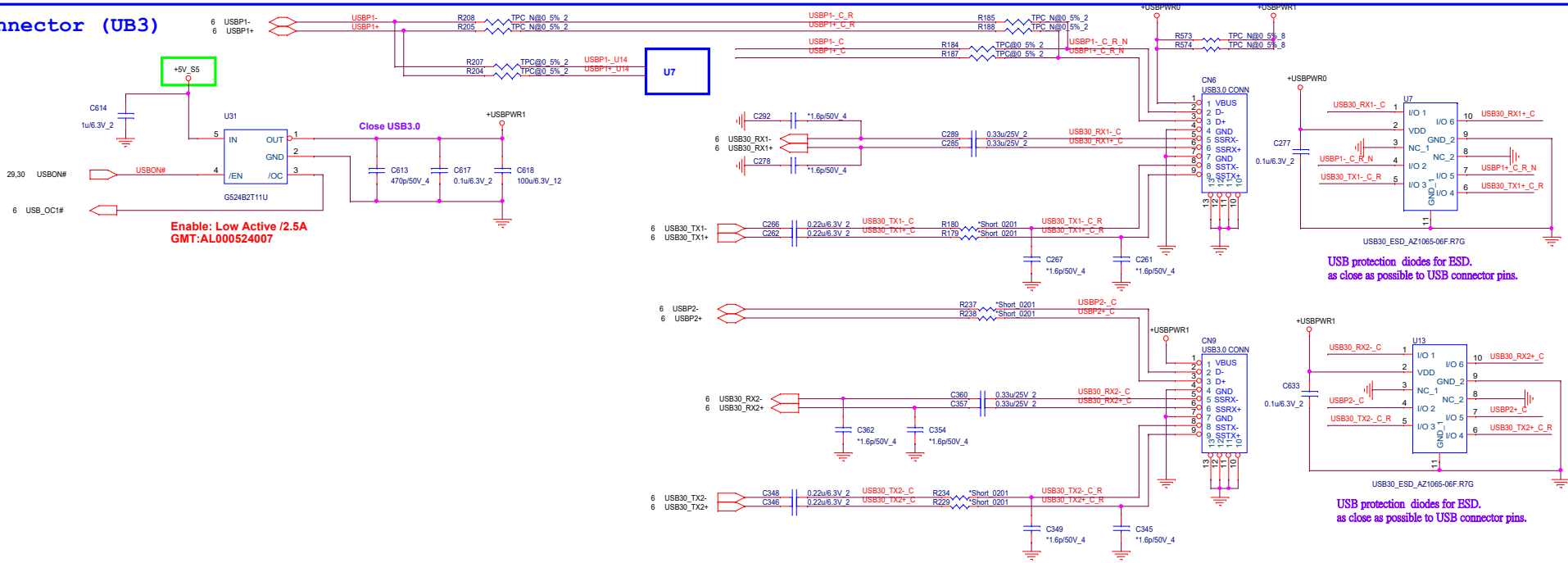


	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

0326 TI AL002544001 (TPS2544RTER)

RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:  
1. ILIM\_SEL is always set high  
2. Load Detection - Port Power Management is not used  
3. Mouse / Keyboard wake function is not used  
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use  
RILIM\_LO < 80.6 kΩ.  
The following equation programs the typical current limit:  
(1)  
$$IOS\_typ(mA) = 50,250 / \{RILIM\_XX(K\Omega) + 0.1\}$$
  
RILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

USB 3.0 Connector (UB3)

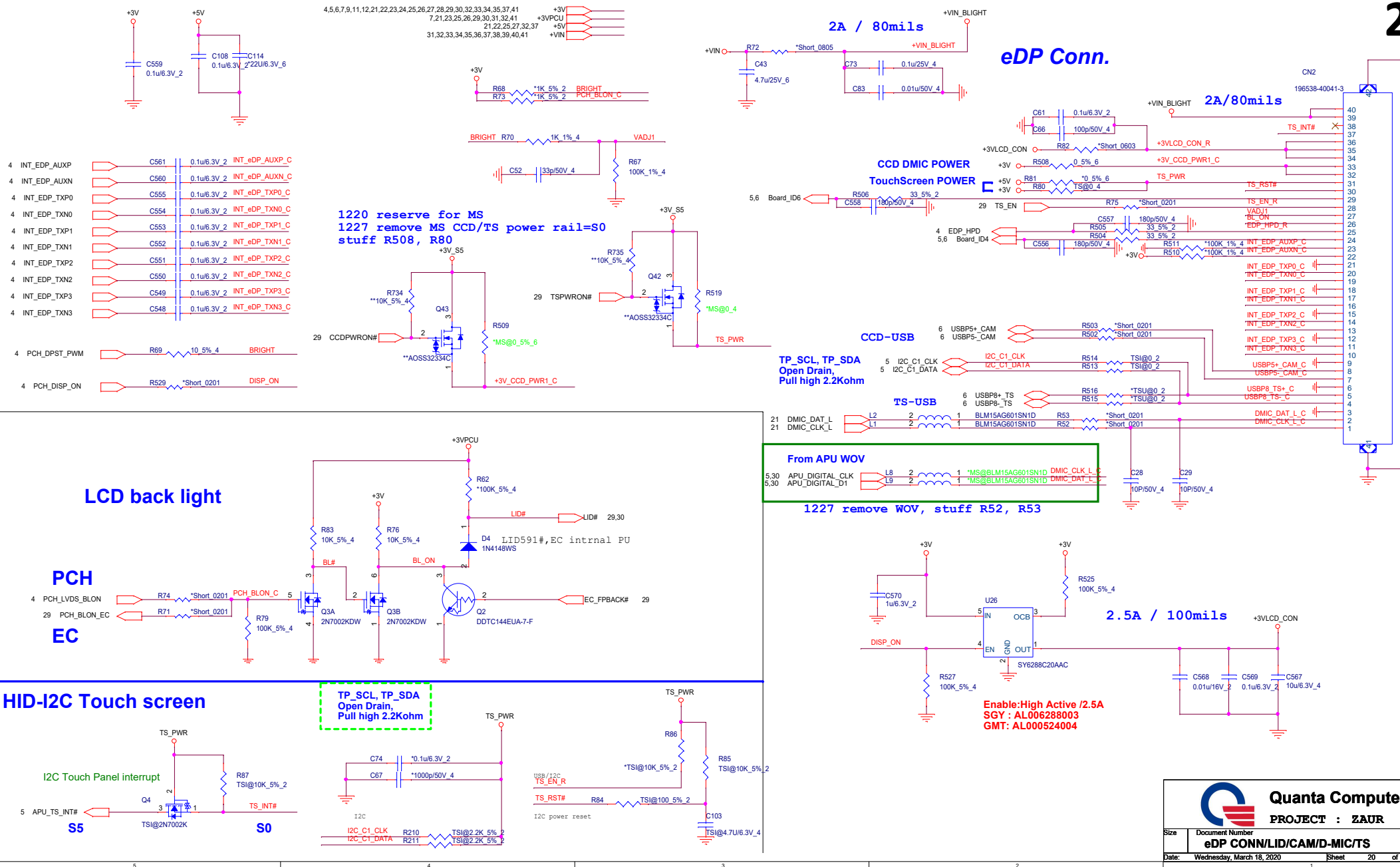


USB protection diodes for ESD,  
as close as possible to USB connector pins.

USB protection diodes for ESD,  
as close as possible to USB connector pins.

CAP close to different CONN



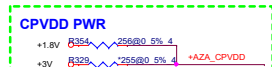


**Quanta Computer Inc.**  
**PROJECT : ZAUR**

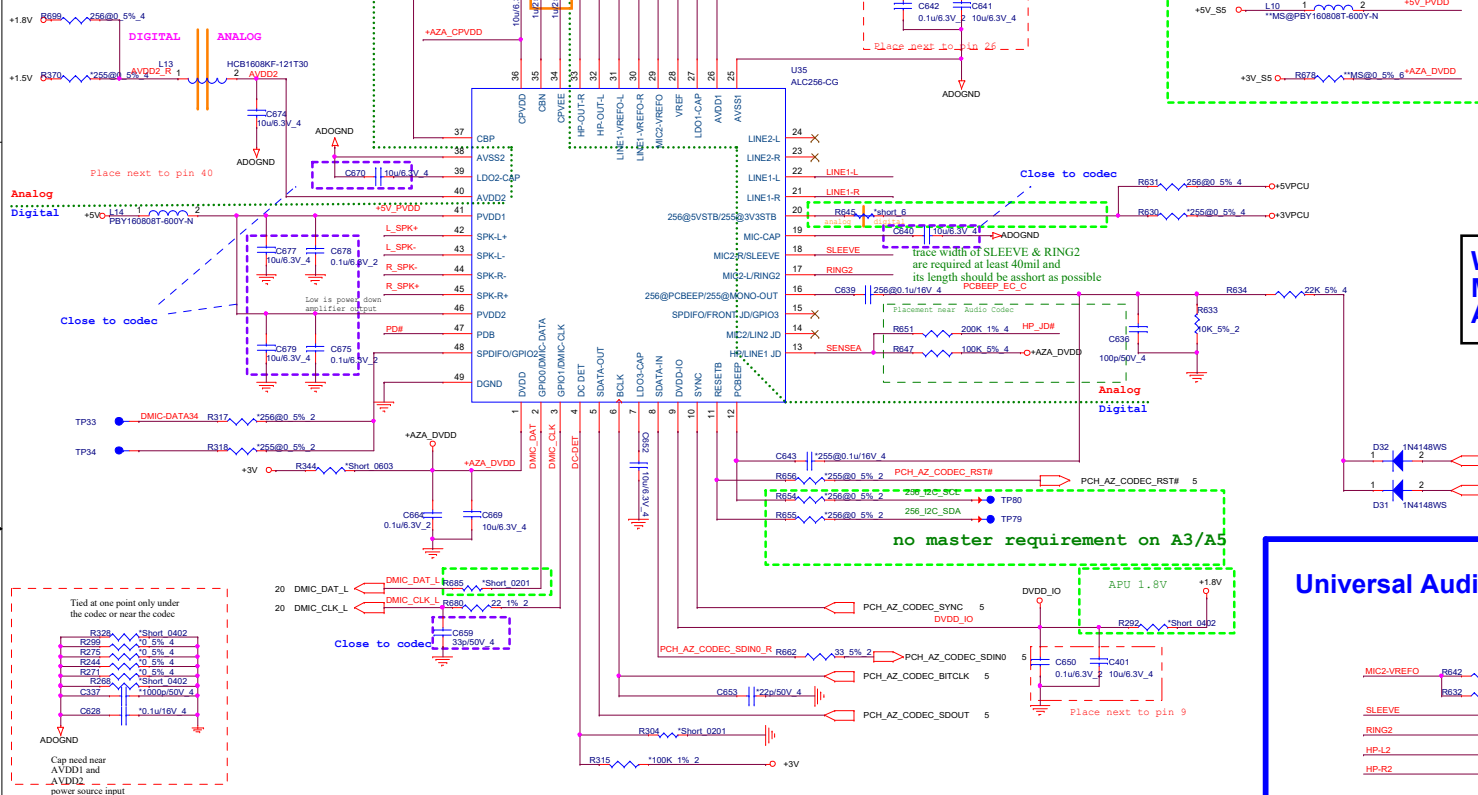
Size	Document Number	Rev
	<b>eDP CONN/LID/CAM/D-MIC/TS</b>	1A
Date:	Wednesday, March 18, 2020	Sheet 20 of 44



## Codec(ADO)



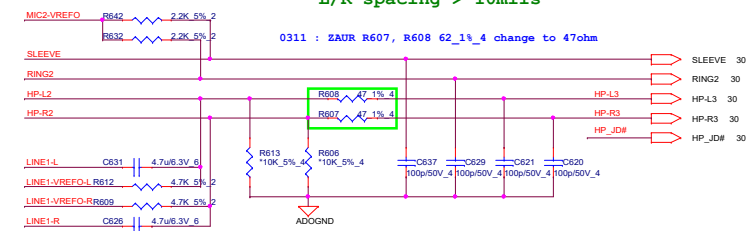
### Codec PWR 1.8V(ADO)



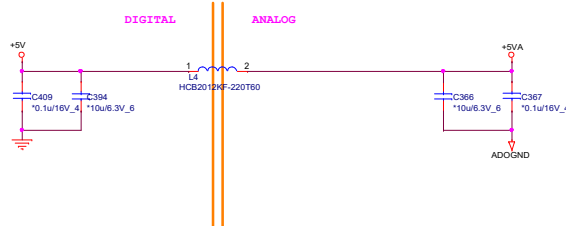
WW G2 @ ALC256 : AL000256009  
MGF G3 @ ALC3256M:  
ALC255 : AL000255000- Design reserved

**Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)**

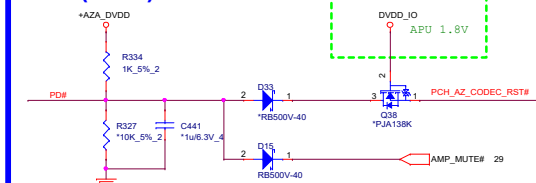
SLEEVE/RING2 trace > 40mils  
HP/LINE trace > 10mils  
L/R spacing > 10mils



### Codec PWR 5V(ADO)



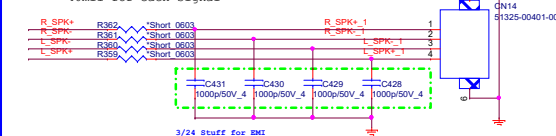
## Mute(ADO)



## Internal Speaker

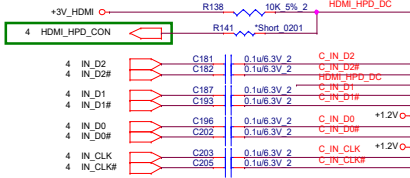
4 ohm : 40mil for each signal

40mil for each signal

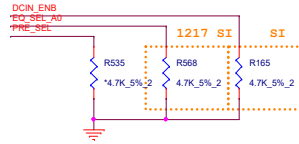
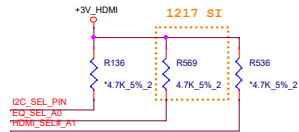




HDMI\_HPD PD100K @ APU side



PS8409 strap pin



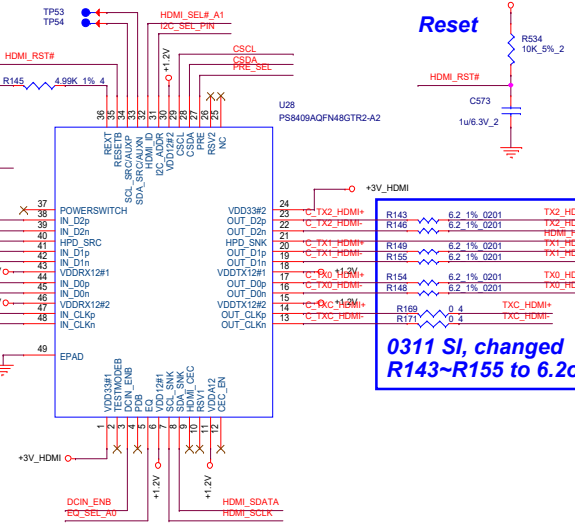
DCIN\_ENB  
DC coupling enable; Internal pull up, 3.3V I/O.  
L: DC coupling input  
H: Default, AC coupling input

EQ\_SEL\_A0  
Receiver equalization setting; Internal pull up, 3.3V I/O.  
L: Compensation for channel loss up to 13dB  
H: Default, Compensation for channel loss up to 17dB  
M: Compensation for channel loss up to 11dB

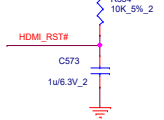
PRE\_SEL  
Output pre-emphasis setting; Internal pull up, 3.3V I/O.  
L: Pre-emphasis =2.5dB  
H: Default, No Pre-emphasis

HDMI\_SEL#\_A1  
HDMI ID enable; Internal pull down, 3.3V I/O.  
L: Default, HDMI ID enable  
H: HDMI ID disable

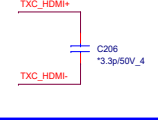
I2C\_SEL\_PIN  
I2C Slave Address selection; Internal pull down, 3.3V I/O.  
L: Default, Slave address 0x10-0x2F.  
H: Alternative slave address 0x90-0x9F, 0xD0-0xDF.



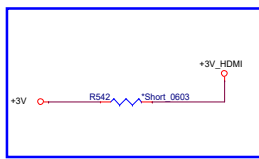
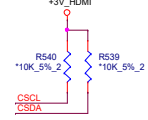
Reset



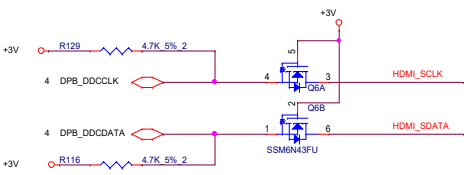
Reserve



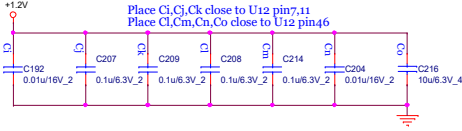
Optional



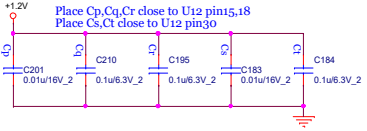
0311 SI, changed R129, R116 to 4.7K



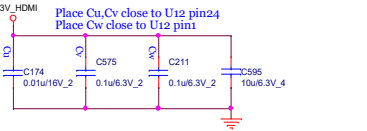
Place Ci,Cj,Ck close to U12 pin7,11  
Place Ci,Cm,Cn,Co close to U12 pin46



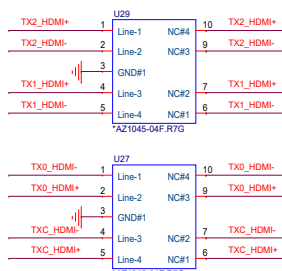
Place Cp,Cq,Cr close to U12 pin15,18  
Place Cs,Ct close to U12 pin30



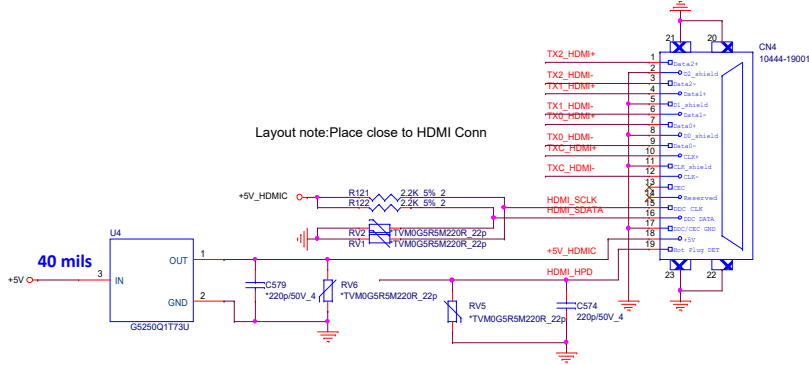
Place Cu,Cv close to U12 pin24  
Place Cw close to U12 pin1



For ESD  
Layout note: Place close to HDMI Conn



Layout note: Place close to HDMI Conn





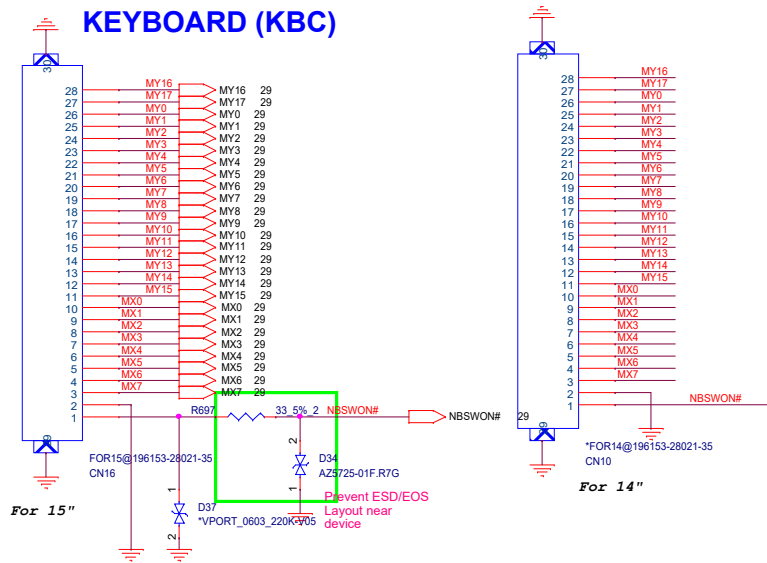






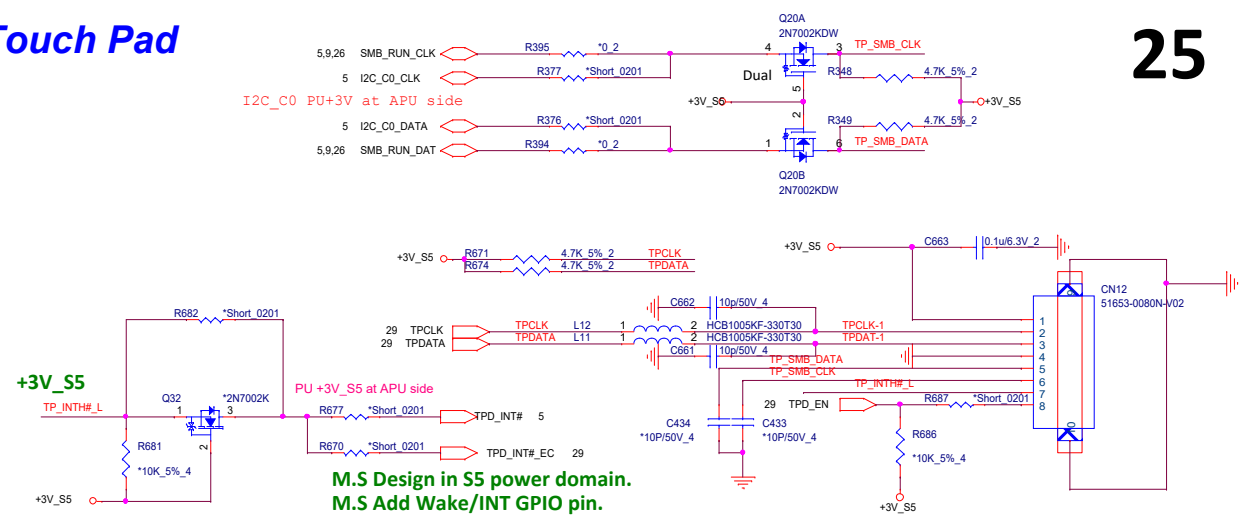


## KEYBOARD (KBC)

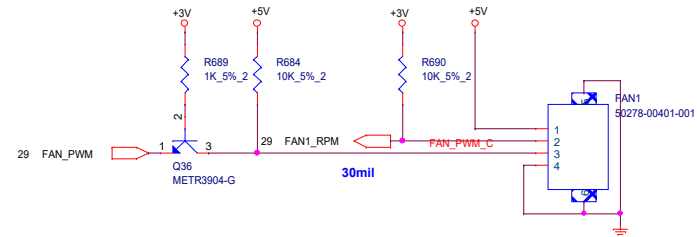


MY5	C468	220p/25V_2
MY6	C469	220p/25V_2
MY3	C466	220p/25V_2
MY7	C470	220p/25V_2
MY8	C471	220p/25V_2
MY9	C472	220p/25V_2
MY10	C473	220p/25V_2
MY11	C474	220p/25V_2
MY1	C464	220p/25V_2
MY2	C465	220p/25V_2
MY4	C467	220p/25V_2
MY0	C463	220p/25V_2
MX4	C688	220p/25V_2
MX6	C690	220p/25V_2
MX3	C687	220p/25V_2
MX2	C686	220p/25V_2
MX7	C691	220p/25V_2
MX0	C684	220p/25V_2
MX5	C689	220p/25V_2
MX1	C685	220p/25V_2
MY12	C475	220p/25V_2
MY13	C476	220p/25V_2
MY14	C477	220p/25V_2
MY15	C683	220p/25V_2
MY16	C461	220p/25V_2
MY17	C462	220p/25V_2

## Touch Pad

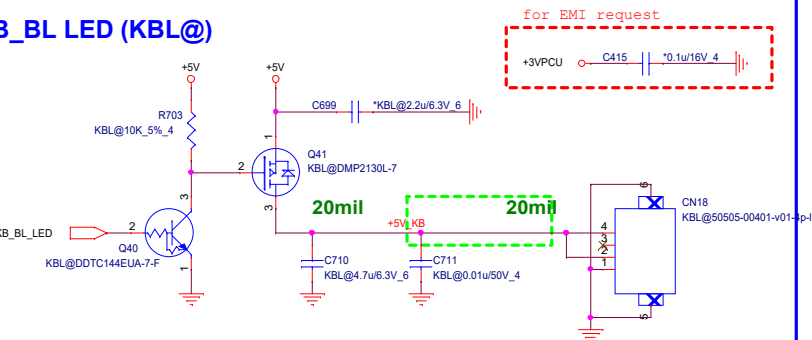


## FAN

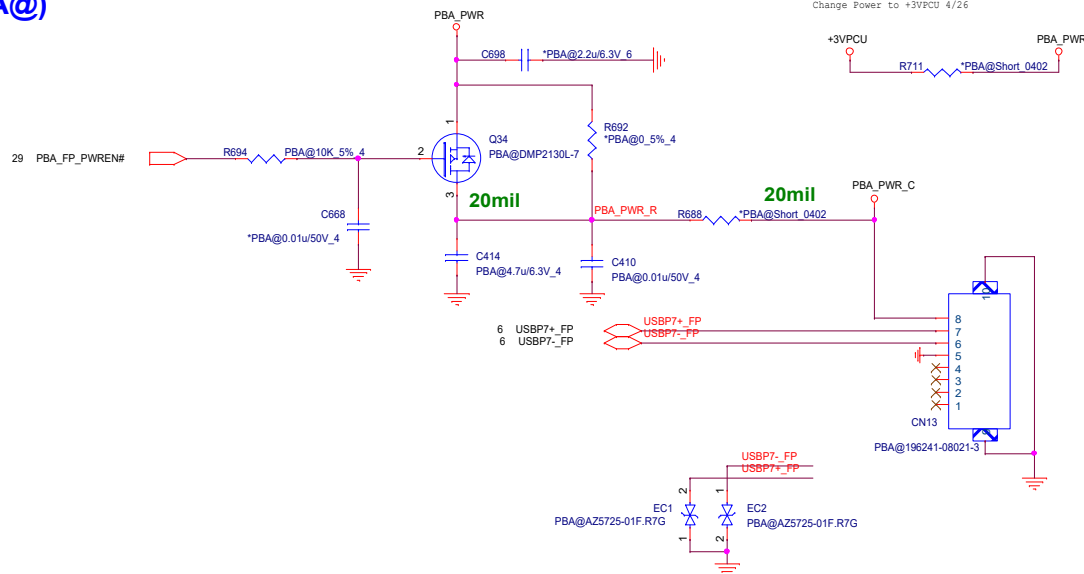


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## KB\_LED (KBL@)









M.S SATA SSD devices should be powered from S5 rail during S0i3, and should support DEVSLP as well as HIPM functionality. The SATA SSD power should be gated by EC GPIO during S3, S4, and S5.

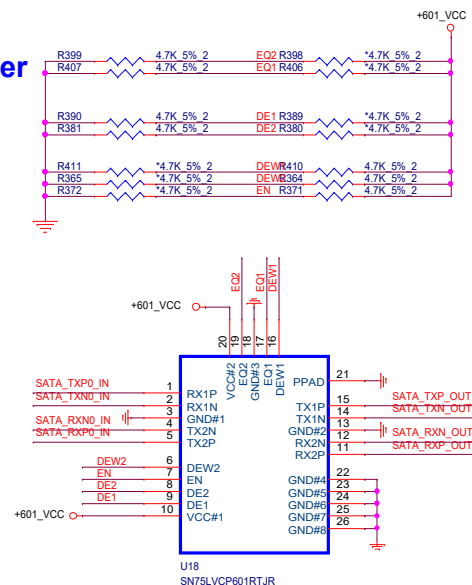
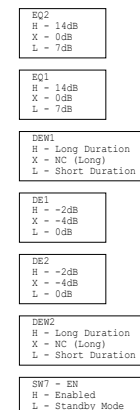
	19,21,24,30,32,34,35,39	+5V_S5
	20,21,22,25,32,37	+5V
4,5,6,7,9,11,12,20,21,22,23,24,25,26,28,29,30,32,33,34,35,37,41		+3V
	5,6,7,11,20,21,23,25,28,29,32,37,38	+3V_S5



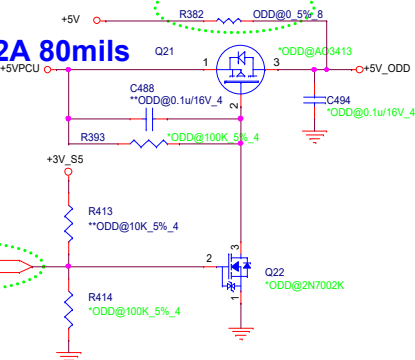
27



## SATA HDD Re-driver



**each power 2A 80mils**



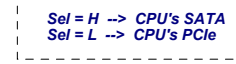
M.S EC assignment reserved  
A3/A5 do not support ODD

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**PROJECT : ZAUR**

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	<b>HDD/ ODD</b>	<b>1A</b>
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Close to conn.

rating = 1000mA @ 128G

2.5A / 100mils



**0301 MS stuff D16 and D17**

WLAN\_PLT\_RST#

D16 2

D17 2

PCIE\_RST# 5, 12, 23, 28

EC\_WLAN\_RST# 29

PERST# rise time < 20ns

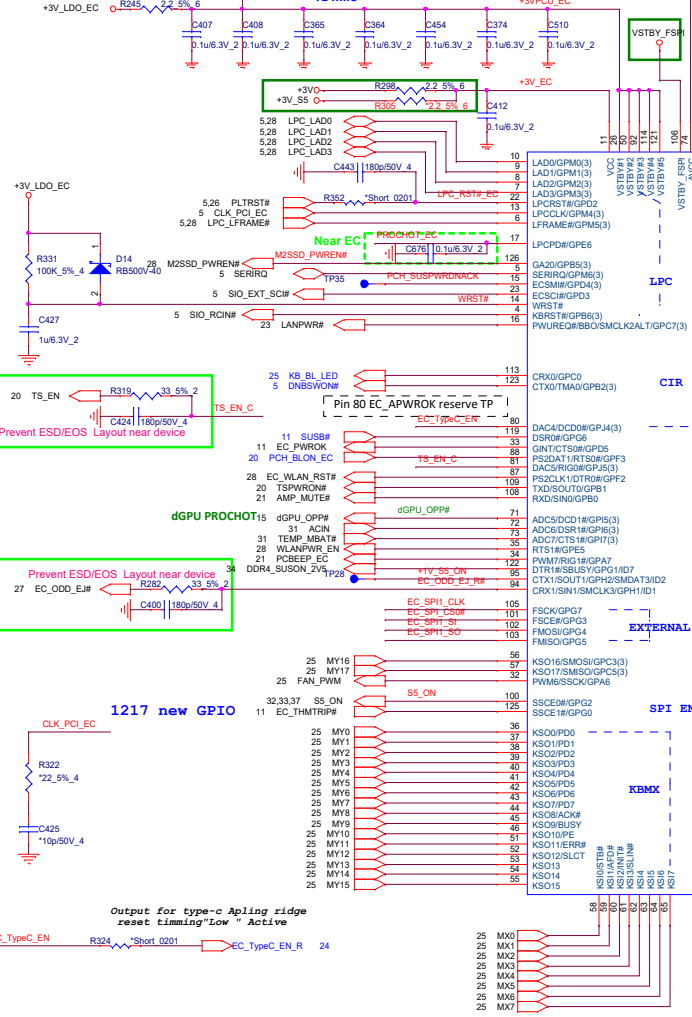
PC WLAN\_RST# for modern standby  
PCIE\_RST# is reserved

5%\_2 1227 BT\_EN changed to APU



# EC(KBC)

+3VPCU\_EC and +3V\_RTC minimum trace width 12mils.



## IT8987E/BX LQFP

Pin 80 EC\_APWROK reserve TP

UART port

EXTERNAL SERIAL FLASH

SPI ENABLE

KBMX

CLOCK

A/D D/A

WAKE UP

Ring#PWRFAIL#CK32CLK0/LPCRTST#GPB7

AD0/GPI0(3)

AD1/GPI1(3)

AD2/GPI2(3)

AD3/GPI3(3)

AD4/GPI4(3)

TACH2/GPJ0(3)

GPJ1(3)

DAC2/TACH0B/GPJ2(3)

DAC3/TACH1B/GPJ3(3)

GPJ4(3)

GPJ5(3)

GPJ6(3)

GPJ7(3)

GPJ8(3)

GPJ9(3)

GPJ10(3)

GPJ11(3)

GPJ12(3)

GPJ13(3)

GPJ14(3)

GPJ15(3)

GPJ16(3)

GPJ17(3)

GPJ18(3)

GPJ19(3)

AJ089870F01 IT8987E/BX

SM BUS ARRANGEMENT TABLE

SM Bus 1 Battery

SM Bus 2 PCHVGA/DDR

SM Bus 3

SM Bus 4

SM Bus 5

SM Bus 6

SM Bus 7

SM Bus 8

SM Bus 9

SM Bus 10

SM Bus 11

SM Bus 12

SM Bus 13

SM Bus 14

SM Bus 15

## BIOS/EC shared ROM(16MB)

EC SPI\_CS0#

EC SPI\_CLK

EC SPI\_S0

EC SPI\_S1

EC SPI\_S2

EC SPI\_S3

EC SPI\_S4

EC SPI\_S5

EC SPI\_S6

EC SPI\_S7

EC SPI\_S8

EC SPI\_S9

1.8V 16MB

MX AK5DFN0Z02

WND AK5DF-0N00

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

## SPI NOR FLASH(128KB) (KBC)

reserve for EC debug

3V3 SPI rom, check PN

for EC rom only

EC SPI\_CS0#

EC SPI\_CLK

EC SPI\_S0

EC SPI\_S1

EC SPI\_S2

EC SPI\_S3

EC SPI\_S4

EC SPI\_S5

EC SPI\_S6

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

APU SPI\_S3 R1

APU SPI\_S4 R1

APU SPI\_S5 R1

APU SPI\_S6 R1

APU SPI\_S7 R1

APU SPI\_S8 R1

APU SPI\_S9 R1

APU SPI\_S10 R1

APU SPI\_CS0# R1

APU SPI\_CLK R1

APU SPI\_S0 R1

APU SPI\_S1 R1

APU SPI\_S2 R1

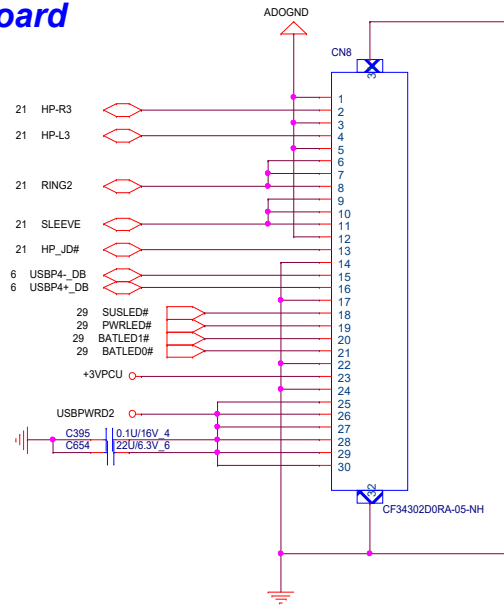
APU SPI\_S3 R1

APU SPI\_S4 R1

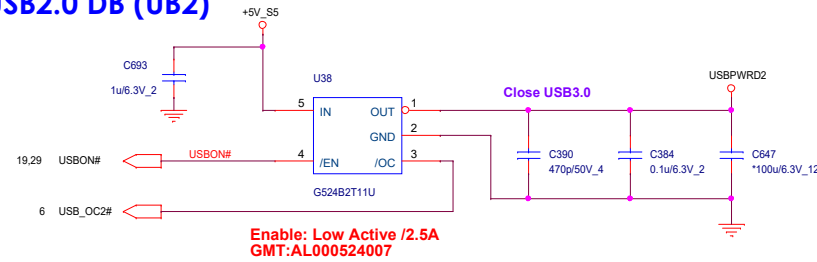
APU SPI\_S5 R1



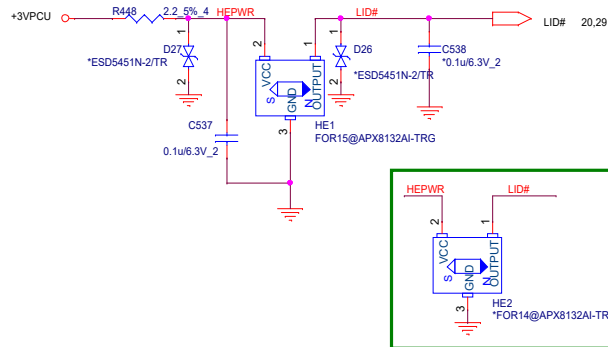
## USB Board



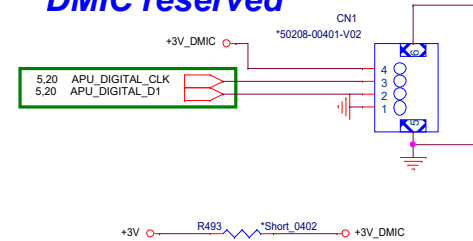
## USB2.0 DB (UB2)



## Hall Sensor



## DMIC reserved

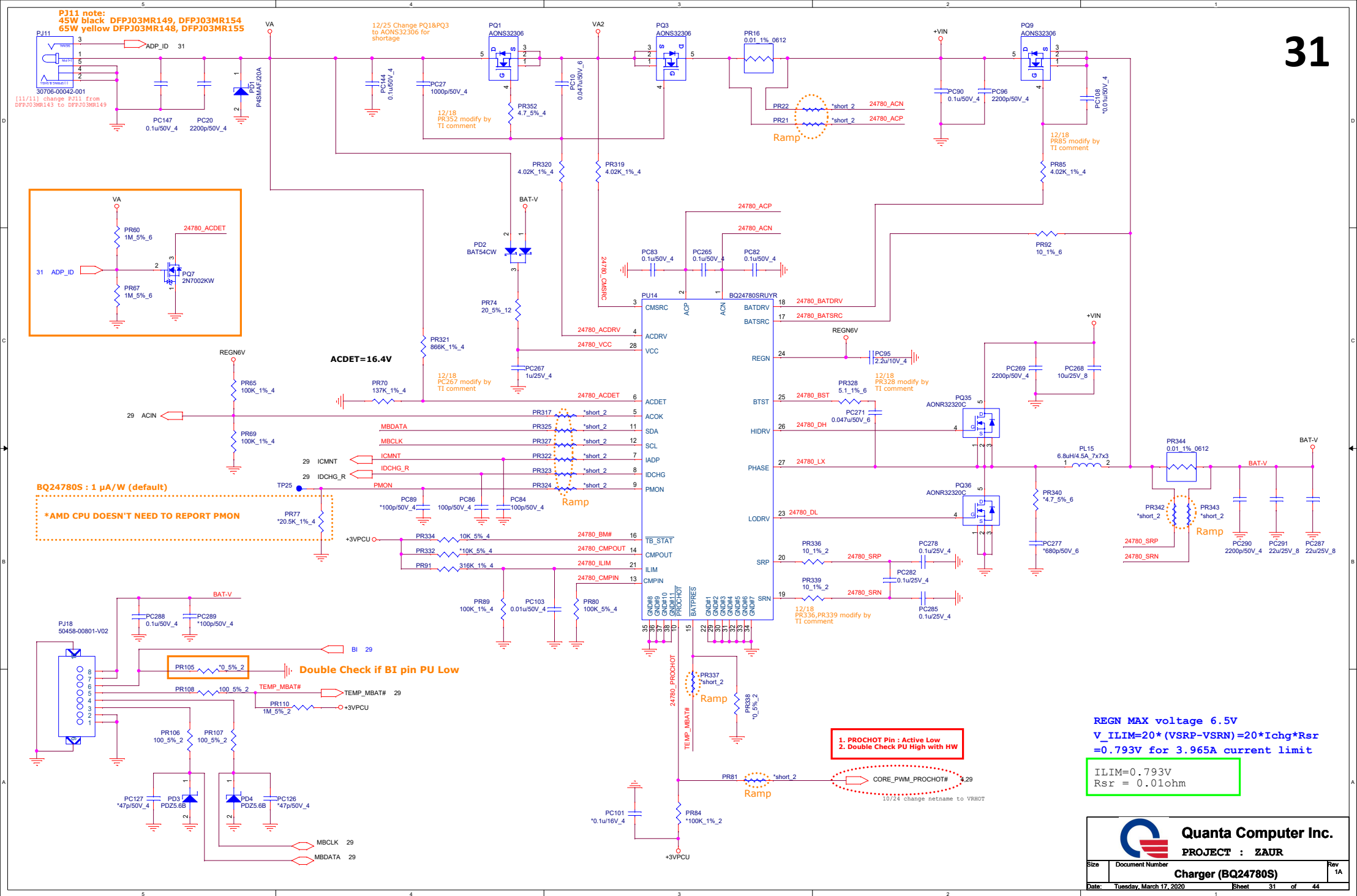


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PROJECT : ZAUR

Size	Document Number	Rev
	USB DB/Hall sensor/DMIC	1A
Date:	Tuesday, March 17, 2020	Sheet 30 of 44

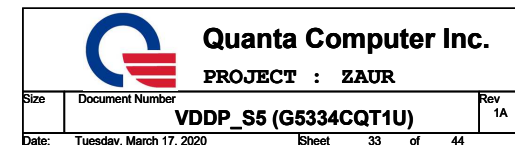




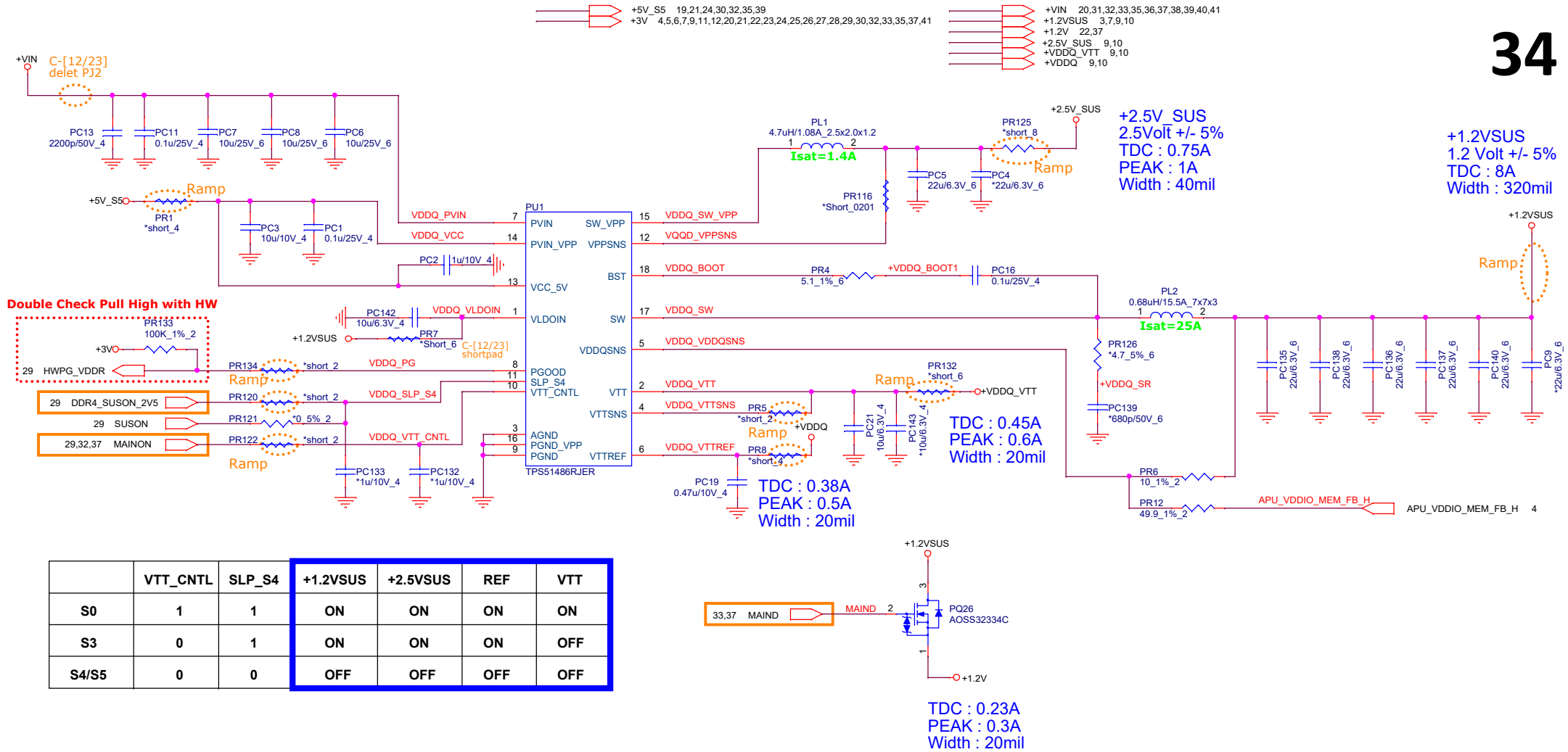












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PROJECT : ZAUR

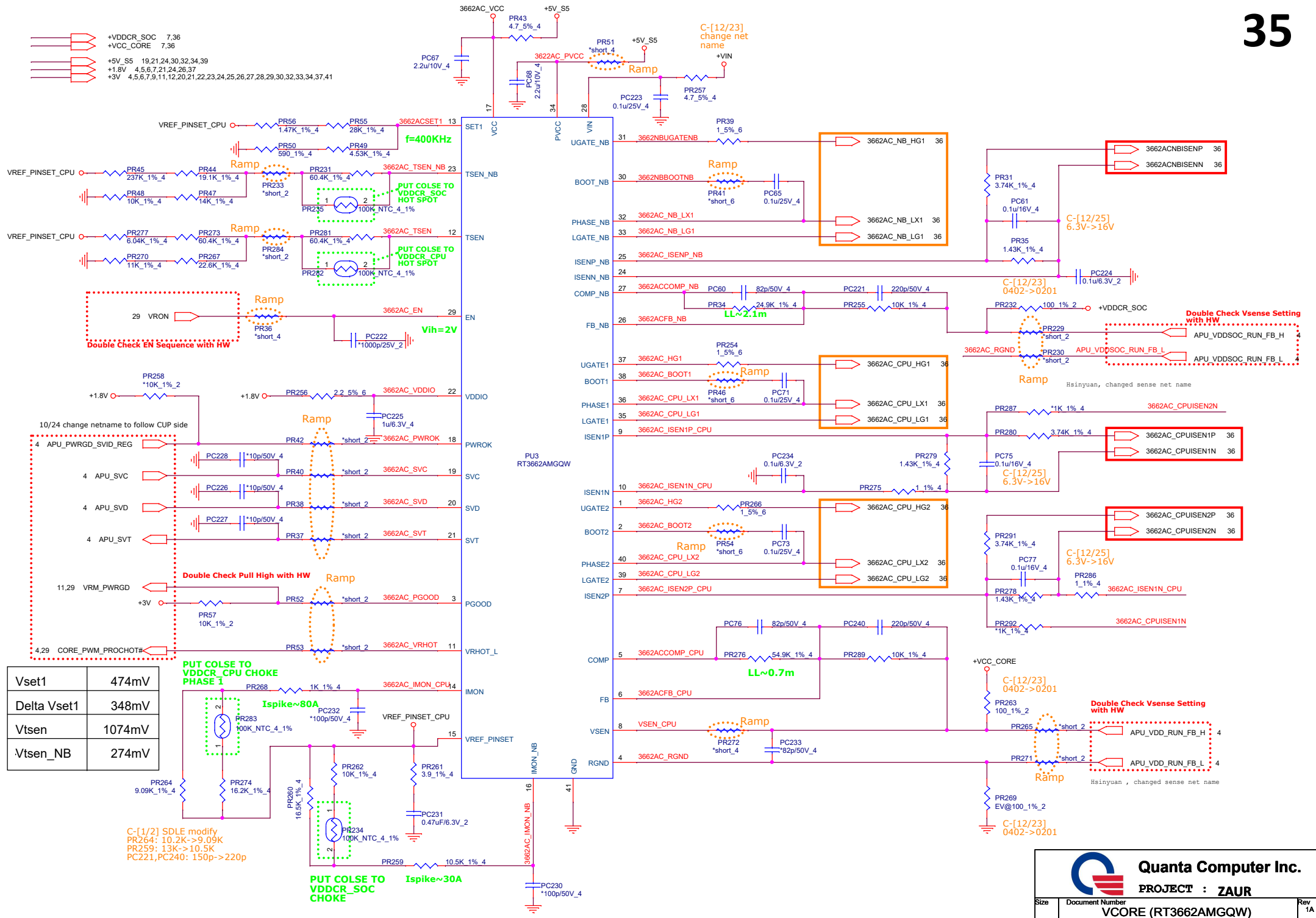
Size	Document Number	Rev
	DDR4_+1.2VSUS (TPS51486R)	1A

Date: Tuesday, March 17, 2020

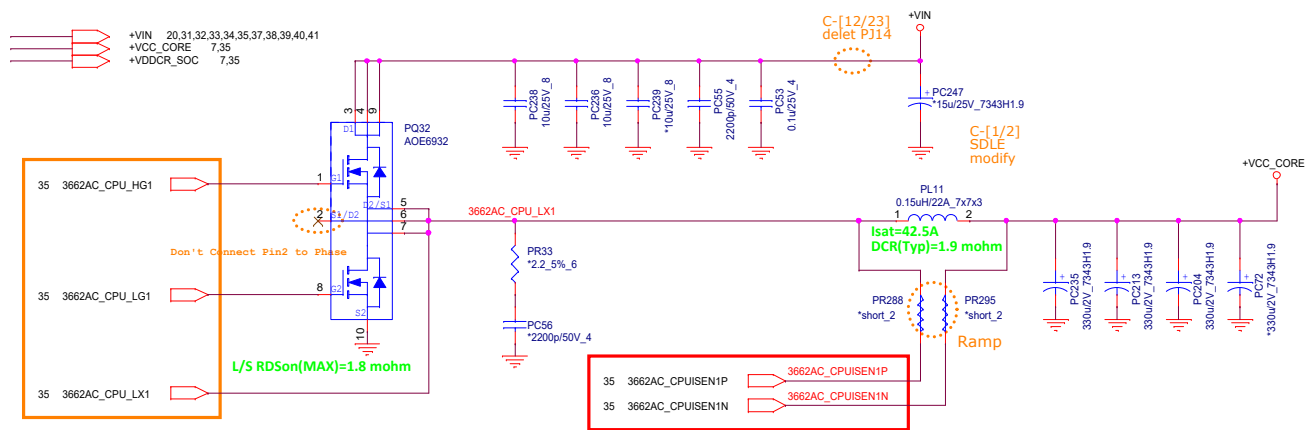
Sheet 34 of 44









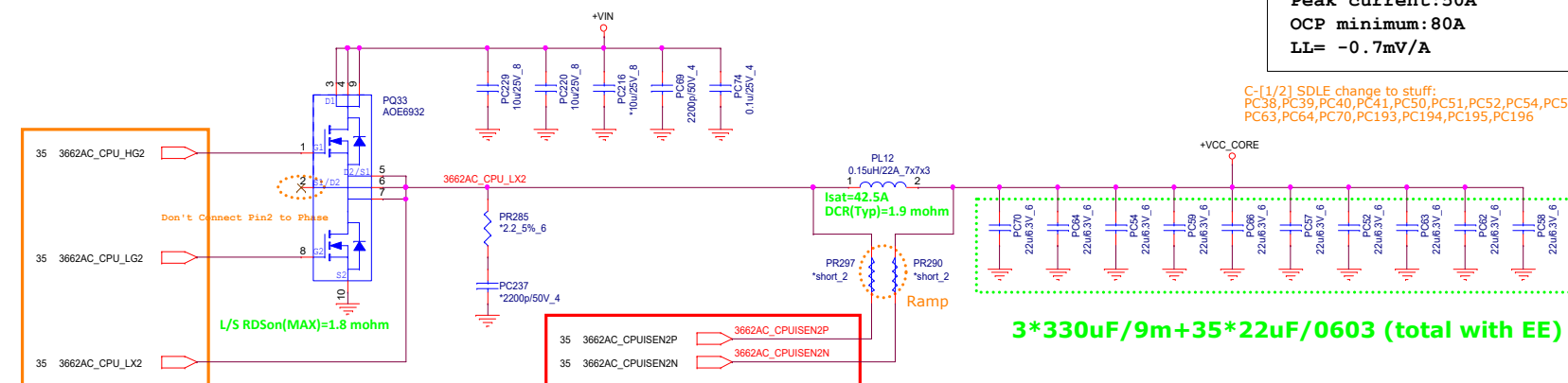
AMD Dali FP5 (15W)

```
VDDCR_VDD
Continue current:35A
Peak current:45A
OCP minimum:80A
LL= -0.7mV/A
```

AMD Renoir FP6 (15W)

```
VDDCR_VDD
Continue current:33A
Peak current:50A
OCP minimum:80A
LL= -0.7mV/A
```

C-[1/2] SDLE change to stuff:  
PC38,PC39,PC40,PC41,PC50,PC51,PC52,PC54,PC59,  
PC63,PC64,PC70,PC193,PC194,PC195,PC196

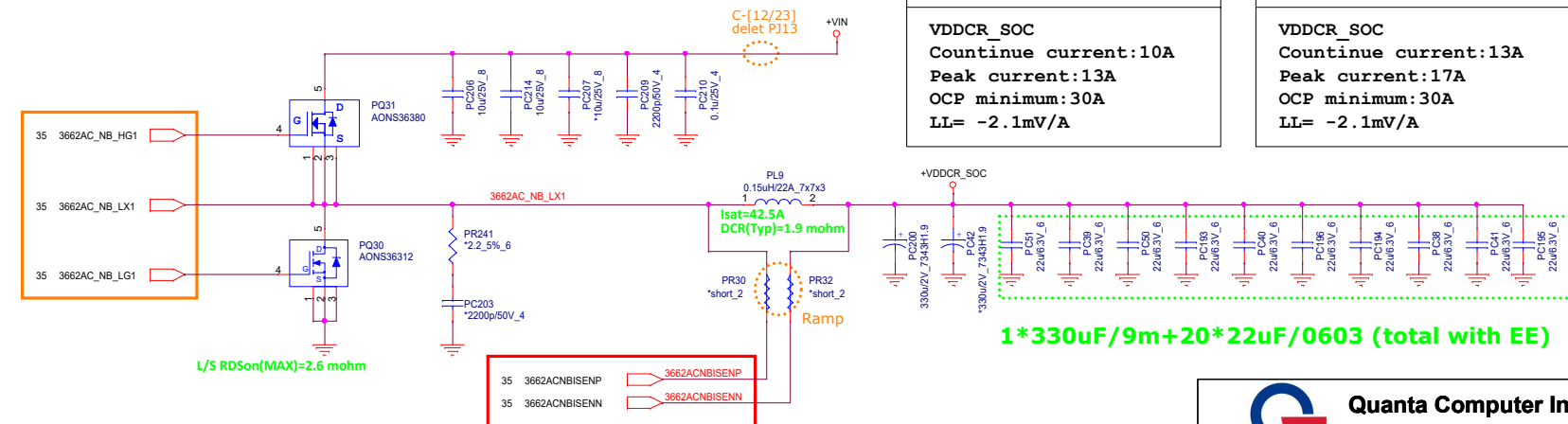


AMD Dali FP5 (15W)

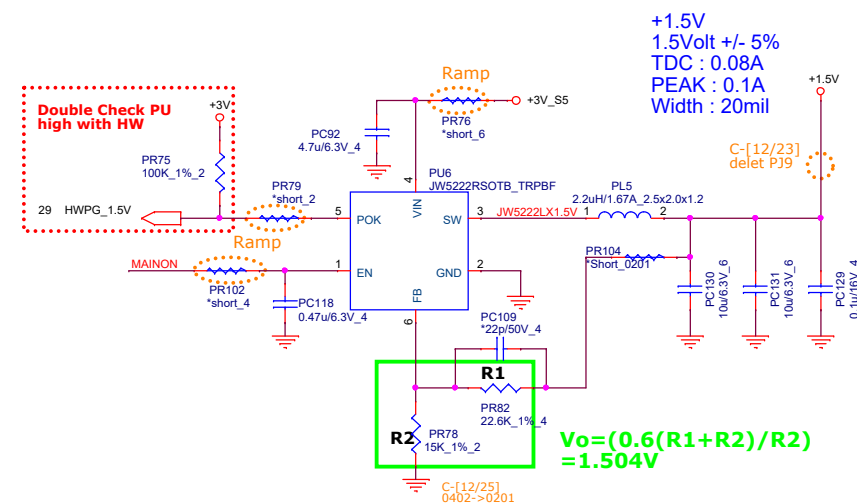
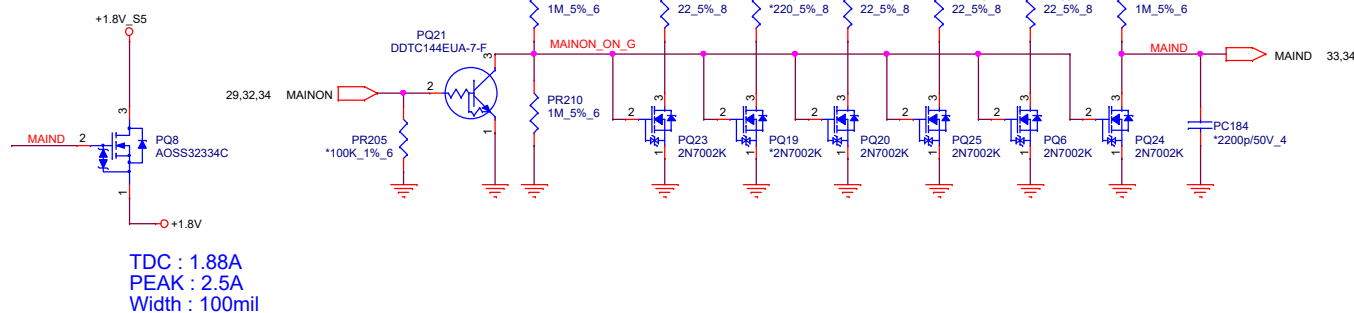
```
VDDCR_SOC
Continue current:10A
Peak current:13A
OCP minimum:30A
LL= -2.1mV/A
```

AMD Renoir FP6 (15W)

```
VDDCR_SOC
Countinue current:13A
Peak current:17A
OCP minimum:30A
LL= -2.1mV/A
```



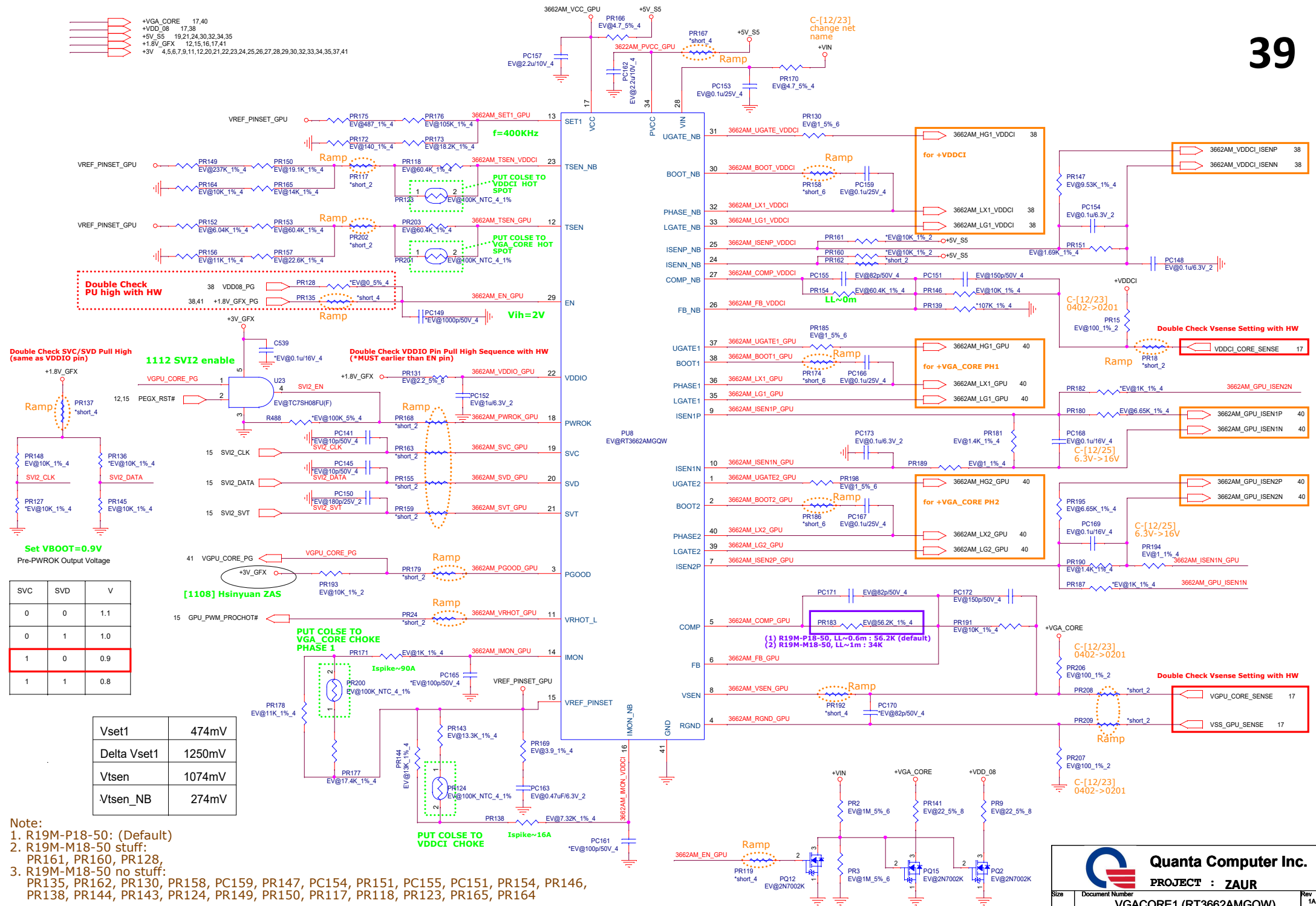


[illegible]

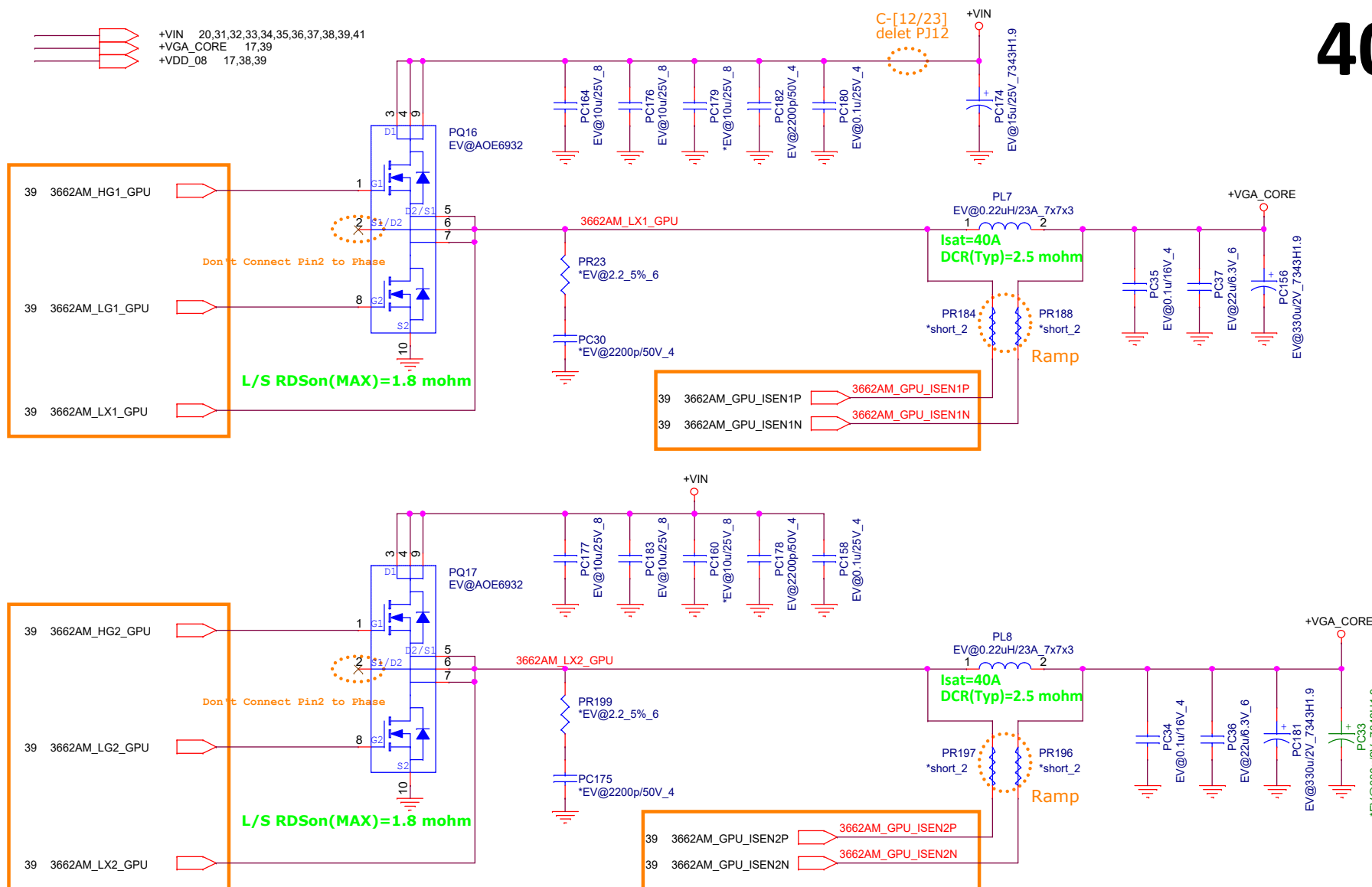












### +VGA\_CORE(R19M-P18-50)\_18W

#### VDDC

TDC : 22A  
 EDC : 60A  
 OCP : 90A  
 LL=-0.6m

### +VGA\_CORE(R19M-M18-50)\_18W

#### VDDC + VDDCI (merged)

TDC : 18A  
 EDC : 60A  
 OCP : 90A  
 LL=-1m



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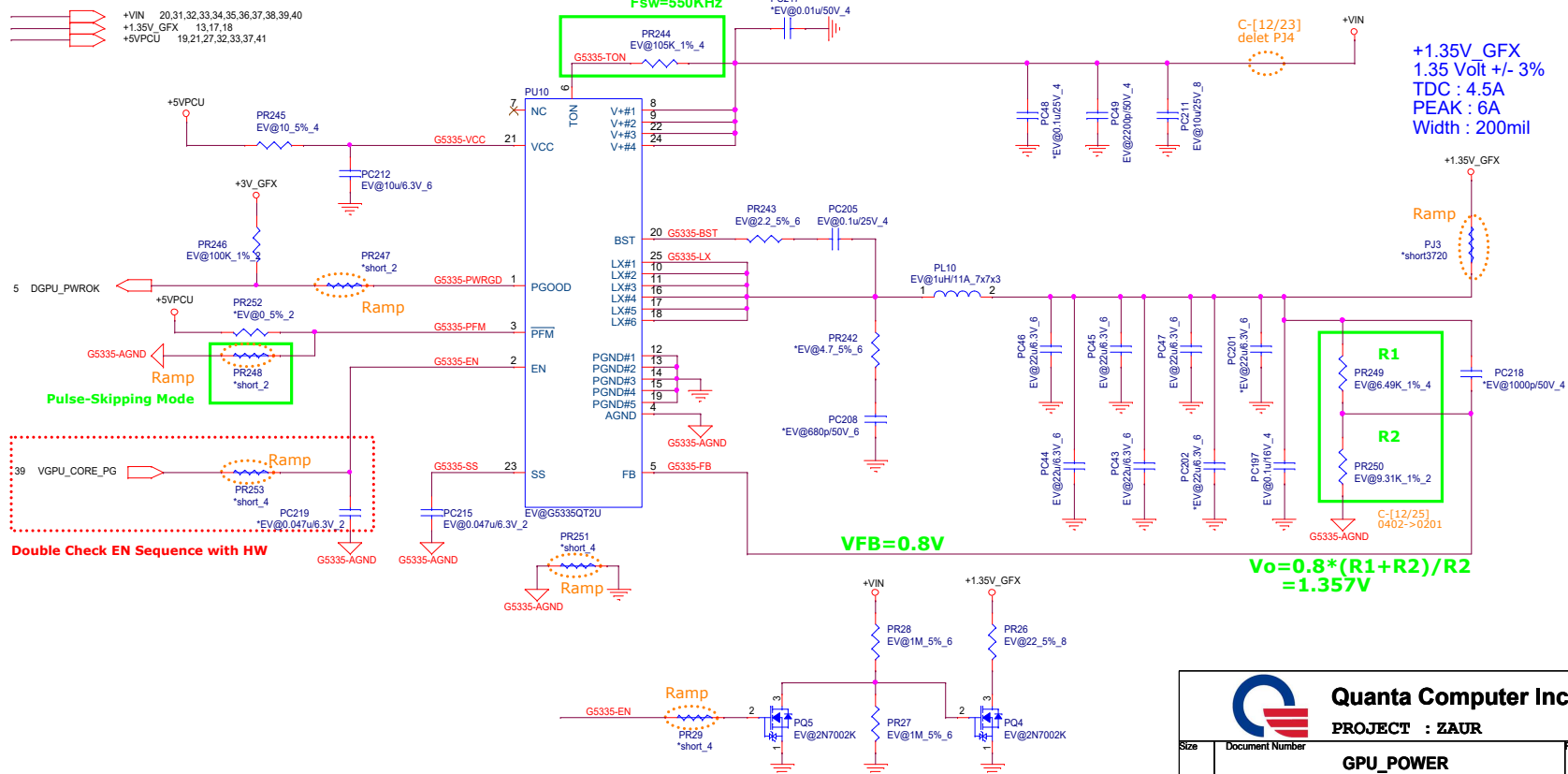
PROJECT : ZAUR

Size Document Number  
VGAORE2 (RT3662AMGQW)

Rev  
1A

Date: Tuesday, March 17, 2020 Sheet 40 of 44

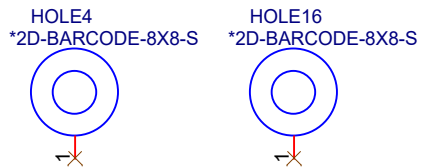
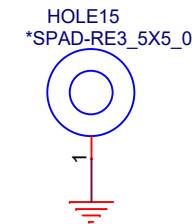
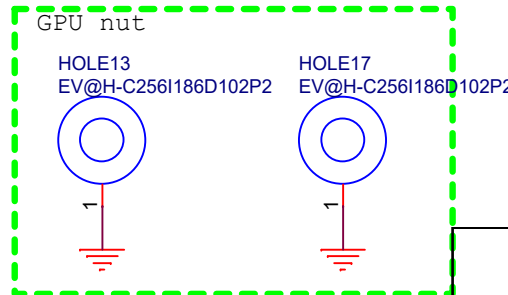
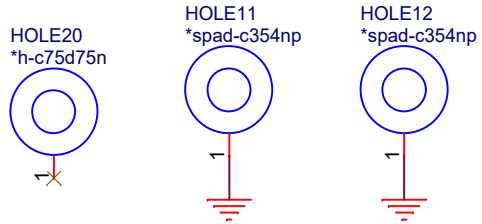
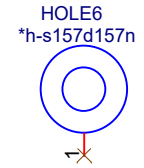
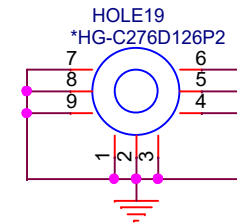
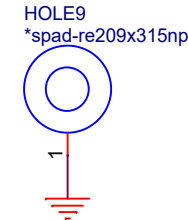
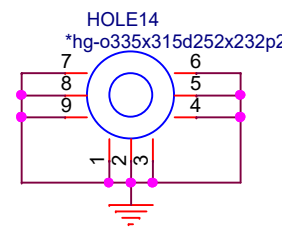
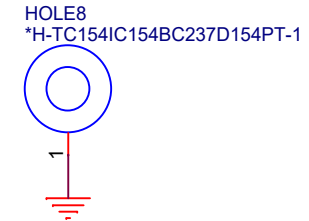
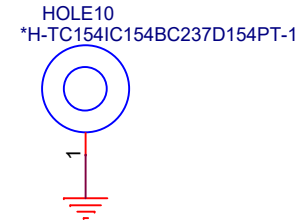
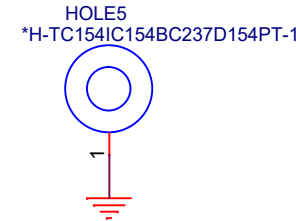
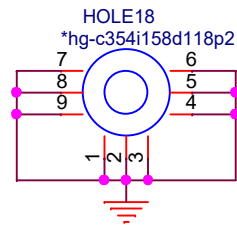
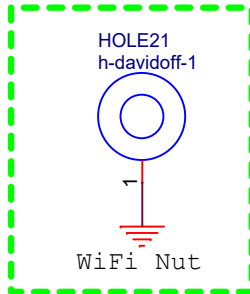
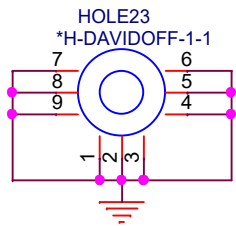
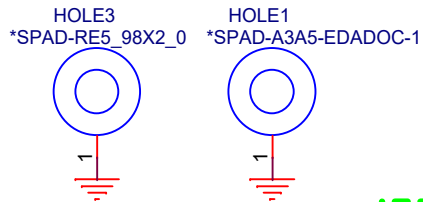
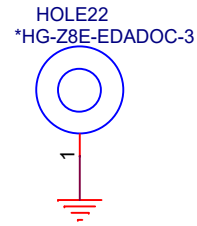
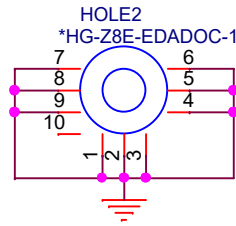






Hole

45

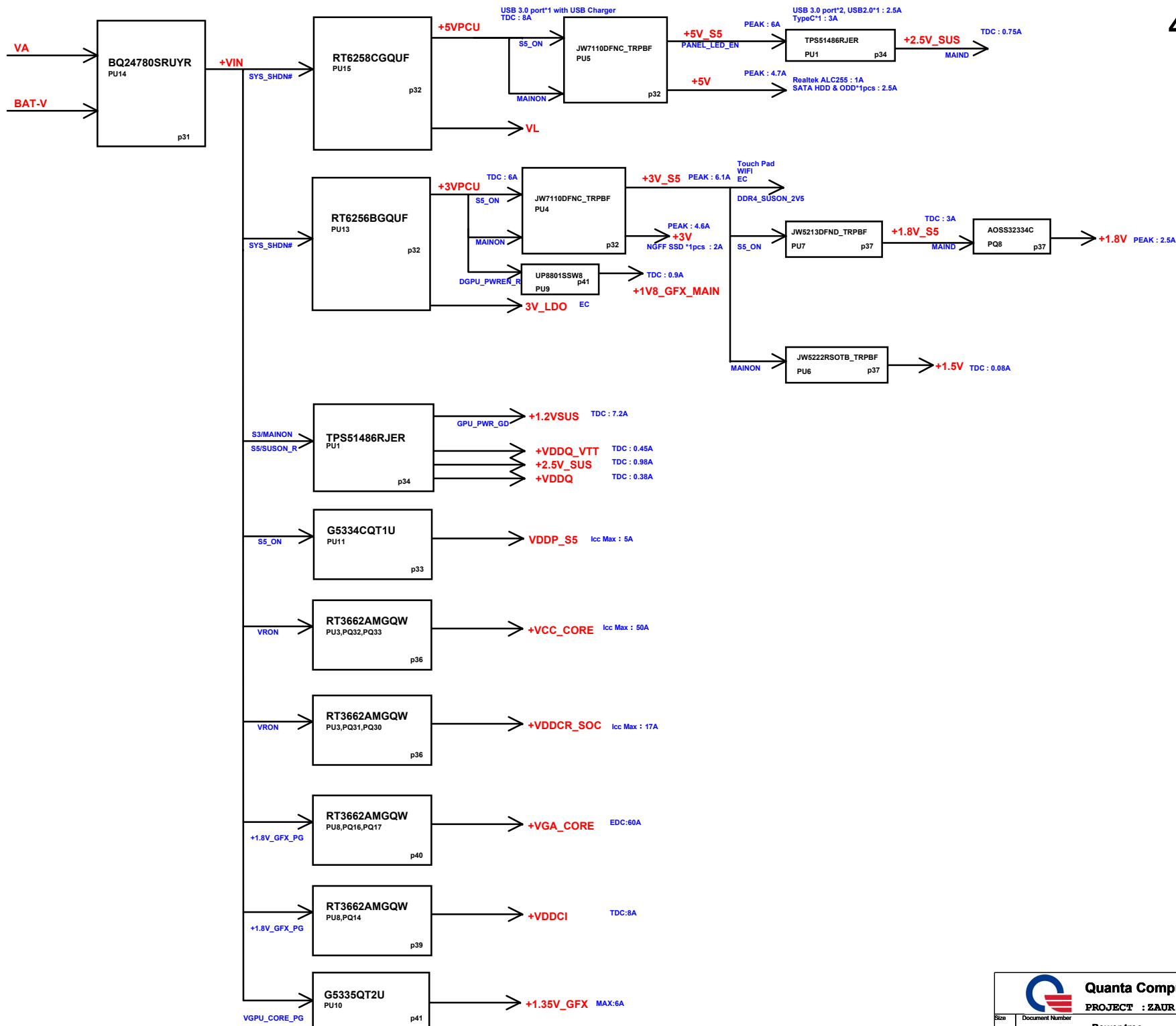


Quanta Computer Inc.

PROJECT : ZAUR

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	Hole	3A
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Stage	Date	CHANGE LIST
A	20191125	1. first released
C	20191217	adjust RAMID by AMD suggestion
		removed hole7
		Stuff R103 make a default low on PEGX_RST#
		Stuff R569 4.7k and R568 4.7k for HDMI2 Eye test pass
		add SDP/DDP bom option
		APU_THERMTRIP# connect to EC new GPIO GPG0 as default, DNS SYS_SHDN# path
		change +1.8V_S5 source to +5VPCU & change +3V_S5 enable to 2ND_S5_ON for Rom sharing
		change U32 to G781-1P8 with slave address 9AH A1000781039
		reserved CCD/DMIC, TSI power gate
		change USB2 ESD protection to BC5V0F1BZ02 *2
		add +VREF_CA1 for MD
	20190317	most 0ohm modified to short pad
		R607/R608 changed to 47 ohm
		PR311 changed to 25.5K
MP		